6.8.3 Real Time Clock Interrupt and Skip Logic

The interrupt and skip logic is used to interrupt the program at a 100 Hz rate.

INT RQST L is asserted when the CLOCK FLAG sets if the CLOCK INTERRUPT ENABLE flip-flop is set. CLOCK INTERRUPT ENABLE is set by DATA11 from the AC being a one when the 6135 instructions is executed by the program. SKIP L is asserted and the program skips an instruction if the CLOCK FLAG sets and 6137 instruction is executed by the program.

6.9 GENERAL PURPOSE PARALLEL I/O BLOCK DIAGRAM DESCRIPTION

The General Purpose Parallel I/O (Figure 6-18) allows the PDP-8/A to transmit or receive one 12-bit word at a time between user designed logic on single ended data lines or two PDP-8/A processors to transfer data to each other, provided each processor has a DKC8-AA I/O option board and the proper cables.

All data transfers are between the AC and an external device via programmed I/O. Data transfer rate is limited by program execution time to approximately 50K words/second.

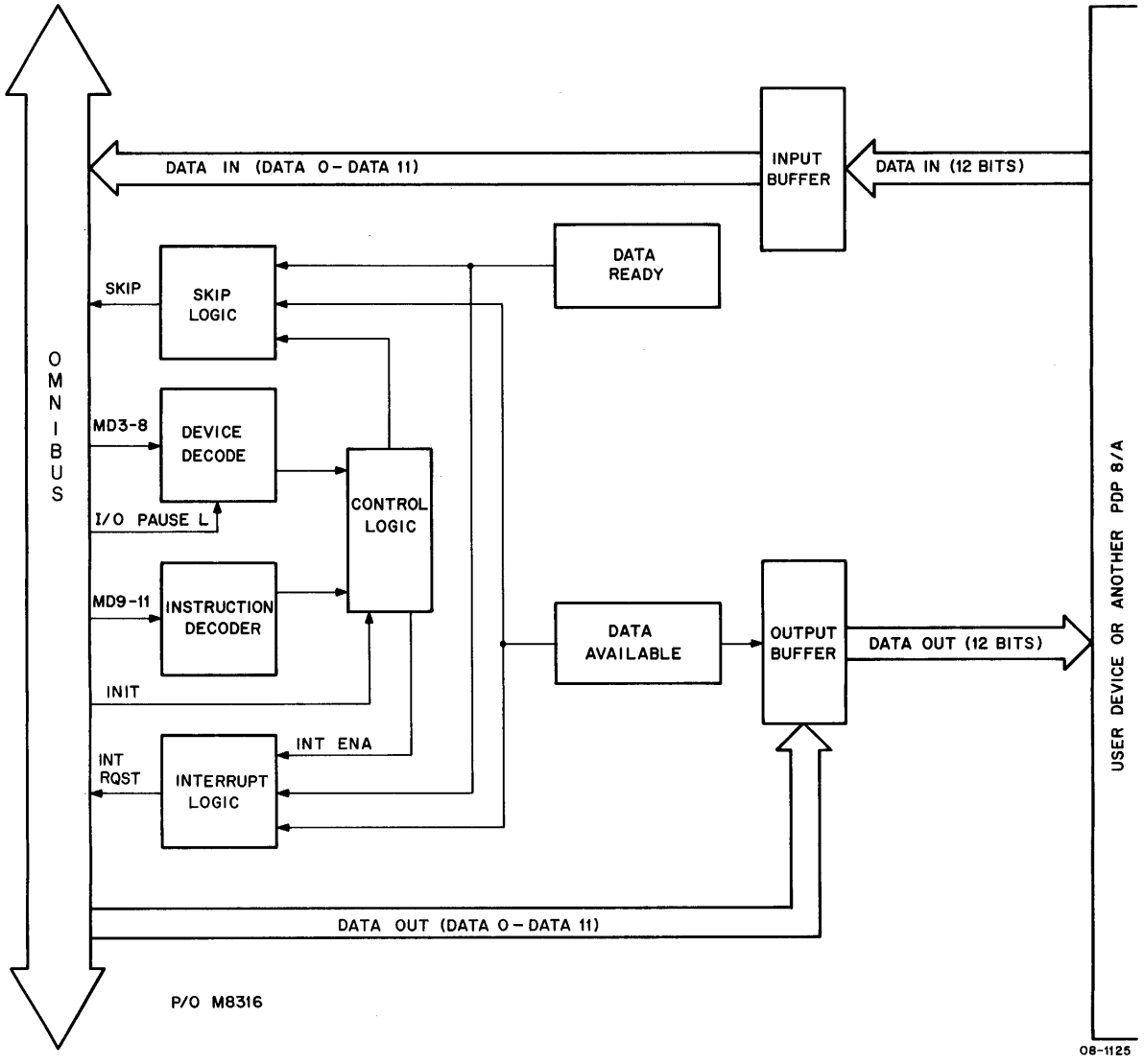

Figure 6-18 General Purpose Parallel I/O Block Diagram

FEATURES

Input/Output:	2 bits of parallel data input and output. Data is logic low true for both transmit and receive operations.
Drive Capability:	Each output drives up to 25 TTL unit loads. Data In presents 4 TTL unit loads to the driver circuit. Maximum cable length is 250 ft for transmit or receive.
Signal Levels:	Logic High is 4.0 V to 2.6 V. Logic Low is 0.0 V to 0.6 V. All signals are TTL compatible.
Cables:	All cables must be ordered separately. The BC08R cable should be used, the standard length is 10 ft, but other lengths up to 250 ft are available on special order. Two cables are needed if both transmit and receive functions are used. The BC80A-0-0 cable in lengths of 25, 50, and 100 ft are available for use with the LA180 printer. Plug the Parallel I/O into Digital standard logic blocks. The use of one or two M9100 cables is required. To transmit data between two PDP-8/A computers, use two BC08R cables. Each cable connects J5 of one DKC8-AA to J4 of the other. The cable must be turned over (connected backwards: pin A is plugged into the pin VV end of the connector) at one end of each cable. (Tables 6-4 and 6-5).

6.10 GENERAL PURPOSE PARALLEL I/O PROGRAMMING

The following instructions are used to program the General Purpose Parallel I/O:

Mnemonic	Octal Code	Function
DBST	6570	Skip on Data Accepted, clear Data Accepted and Data Available, if Data Accepted flag is set.
DBSK	6571	Skip on Data Ready flag.
DBRD	7572	Read data in to AC0-AC11.
DBCF	6573	Clear Data Ready flag, issue Data Accepted out pulse.
DBTD	6574	Load AC0-AC11 into buffer and transmit data out.
DBSE	6575	Set interrupt enable to a 1.
DBCE	6576	Reset interrupt enable to a 0.
DBSS	6577	Issue a strobe pulse.

6.11 DETAILED LOGIC DESCRIPTION

The General Purpose Parallel I/O logic is divided into functional groups for discussion purposes. The block diagram in Figure 6-18 should be used to understand the relationship between the groups of logic.

6.11.1 Device Select and Operations Decoder

The device select and operations decoder logic is shown in Figure 6-19. Bits MD3 – MD8 are gated by I/O PAUSE L when a 657X instruction is decoded to enable the operations decoder and assert INTERNAL I/O L. INTERNAL I/O L causes the positive I/O bus interface to ignore this instruction.

The operations decoder (E25) decodes MD9 – MD11 to determine what operation is to be performed by the parallel I/O. E25 is a BCD to decimal decoder which decodes the 3 bits and asserts one of the output pins to represent instructions 6571 through 6577. When a 6752 instruction is decoded, C0 L and C1 L are asserted (low) to allow data to be transferred from the Data Bus to the AC.

Table 6-4
J4 Input Signal Pin Assignments

Fingers M9100	J1	DKC8-AA J4 Pin No.	Signal Name	Comments
D1	SS	D	STROBE L	450 ns control pulse drives 10 unit loads.*
F1	PP	F	Not used	
J1	MM	J	Not used	
L1	KK	L	DATA IN 0 L	Most significant bit.
N1	HH	N	DATA IN 1 L	Input data low is true.**
R1	EE	R	DATA IN 2 L	
S1	CC	T	DATA IN 3 L	
V1	AA	V	Not used	
U1	Y	X	SET DATA READY L	Low when input data is valid.
U2	W	Z	DATA ACCEPTED OUT L	Low when input data is accepted. Drives 25 unit loads.*
C1	U	BB	Not used	
D2	S	DD	DATA IN 4 L	
F2	P	FF	DATA IN 5 L	
J2	M	JJ	DATA IN 6 L	
L2	K	LL	DATA IN 7 L	Input data, low is true.**
N2	H	NN	DATA IN 8 L	
R2	E	RR	DATA IN 9 L	
T2	C	TT	DATA IN 10 L	
V2	A	VV	DATA IN 11 L	Least significant bit.

All unspecified pins are ground.
*Unit load = 1.6 mA @ logic low and 0.04 mA @ a logic high.
**Presents 4 unit loads to the drive circuit.

Table 6-5
J5 Output Signal Pin Assignments

Fingers M9100	J1	DKC8-AA J5 Pin No.	Signal Name	Comments
D1	SS	D	Not used	
F1	PP	F	Not used	
J1	MM	J	Not used	
L1	KK	L	DATA OUT 0 L	Most significant bit.
N1	HH	N	DATA OUT 1 L	
R1	EE	R	DATA OUT 2 L	Output data, low is true.**
S1	CC	T	DATA OUT 3 L	
V1	AA	V	Not used	
U1	Y	X	DATA AVAILABLE L	Low when output data is valid.
U2	W	Z	DATA ACCEPTED IN L	Low when output data is accepted. Presents 4 unit loads to the driver circuit.*
C1	U	BB	Not used	
D2	S	DD	DATA OUT 4 L	
F2	P	FF	DATA OUT 5 L	
J2	M	JJ	DATA OUT 6 L	
L2	K	LL	DATA OUT 7 L	Output data, low when true.**
N2	H	NN	DATA OUT 8 L	
R2	E	RR	DATA OUT 9 L	
T2	C	TT	DATA OUT 10 L	
V2	A	VV	DATA OUT 11 L	Least significant bit.

Pins A, B, C, E, H, K, M, P, S, U, W, Y, AA, CC, EE, HH, KK, MM, PP, and SS are grounded.
*1 unit load.
**Each output can drive 25 unit loads.

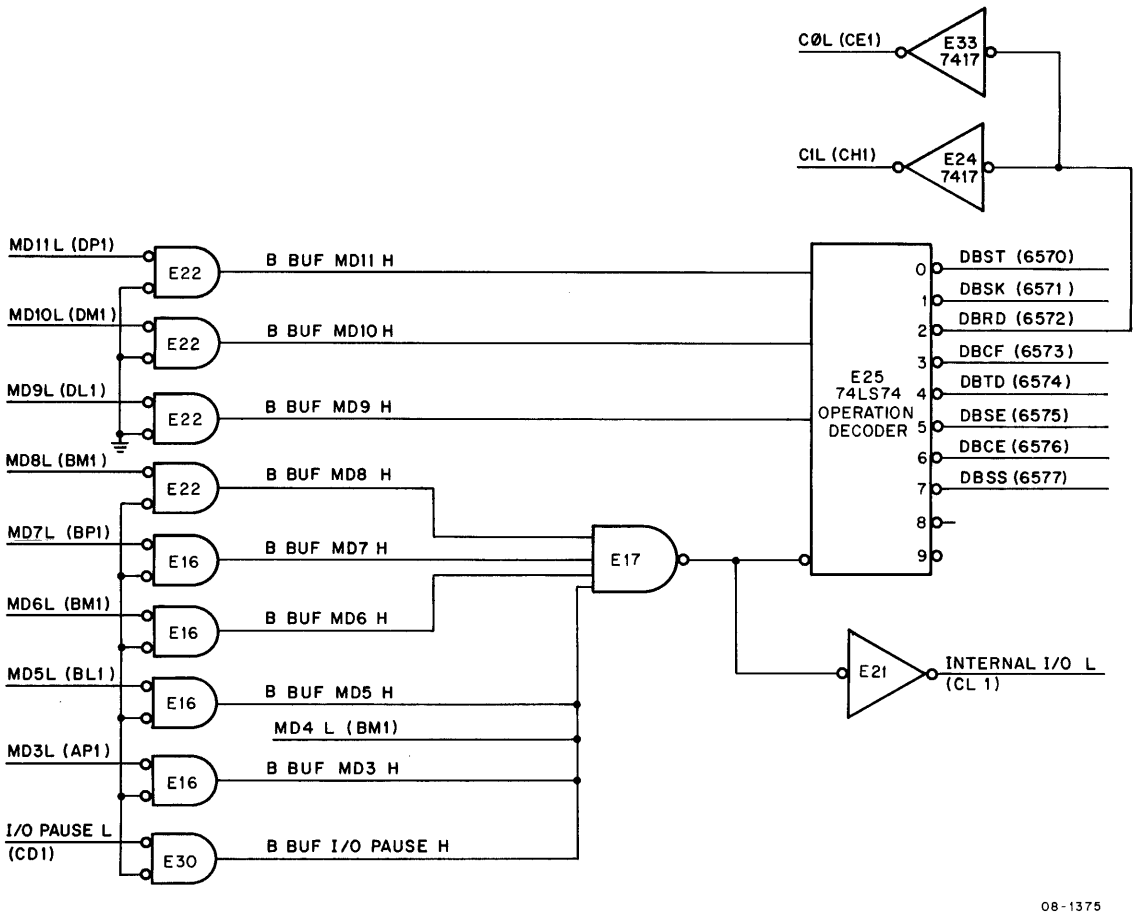

Figure 6-19 Parallel I/O Device Select and Operation Decoder

6.11.2 Interrupt and Skip Logic

The interrupt and skip logic is used to interrupt the program when a data transfer is required. To allow an interrupt to occur, INT ENA must be set by the 6575 instruction. The one output of INT ENA allows INT RQST L to be asserted when DATA READY or B DATA IN sets. SKIP L is asserted if the 6571 instruction is decoded and B DATA IN is set, or if the 6570 instruction is decoded and DATA READY is set. (See the transmit and receive operations in paragraph 6.11.3 for operation of these flags.)

6.11.3 Receive and Transmit Operations

The receive and transmit operations are described separately in the following paragraphs.

6.11.3.1 Transmit Operation – To transmit a 12-bit data word perform the following:

1. Load the output buffer by use of IOT 6574 (Figure 6-20). Data will be transferred from the data lines on the bus into the buffer at TP3 time.

2. At the trailing edge of TP3, DATA AVAILABLE becomes true (low) on the output cable (Figure 6-20). There is a switch on the M8316 that will cause DATA AVAILABLE to be negated (go high) on the leading edge of the next TS1 pulse, if this is desired. This yields a pulse of about 450 ns in duration on the DATA AVAILABLE signal line. The trailing edge of the pulse, on DATA AVAILABLE, could be used to strobe the output data of the M8316 into the user's register. If TS1 is not used to negate DATA AVAILABLE, IOT 6570 (DBST) should be used to negate DATA AVAILABLE.

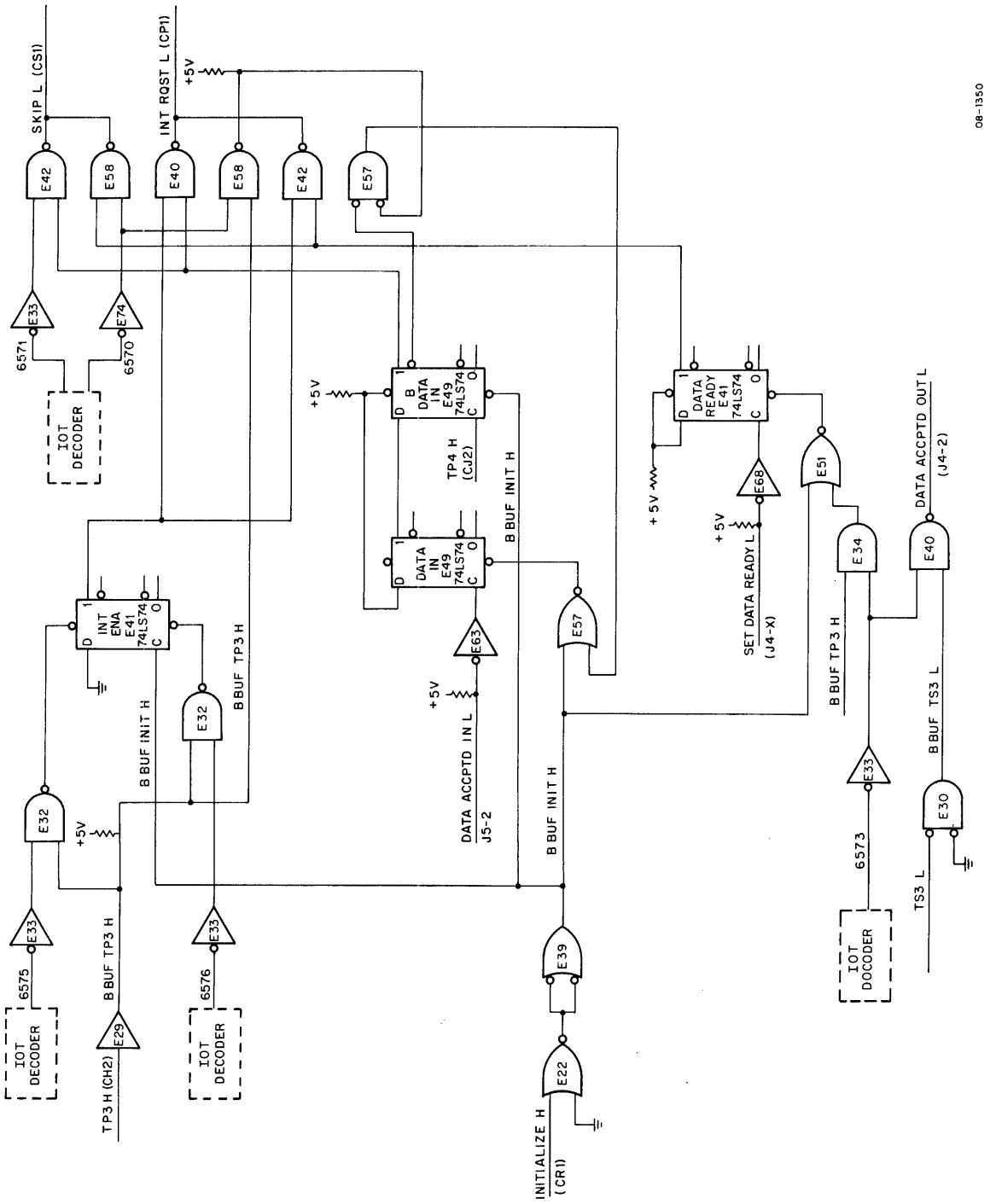

Figure 6-20 General Purpose Parallel I/O Interrupt and Skip Logic

3. The receiving device should then ground DATA ACCEPTED IN to signal the CPU that the transmitted data has been received.

4. Assuming interrupt enable is true, the DATA ACCEPTED flip-flop will assert INT RQST L on the bus. (Figure 6-20).

5. The CPU then executes IOT 6570 to test the DATA ACCEPTED flip-flop and to clear both DATA AVAILABLE and DATA ACCEPTED flip-flops. At TP3 of IOT 6570, DATA AVAILABLE will go high on the output cable. This signals the end of the transmit sequence.

6.11.3.2 Receive Operation – The receive sequence is as follows:

1. The external device places data in some type of latching register then grounds the SET DATA READY line on the input cable which raises the DATA READY flag. (Figure 6-20).

2. Assuming INTERRUPT ENABLE is true, INT RQST L will be asserted on the bus.

3. The CPU then executes the 6571 IOT to test the DATA READY flip-flop; then IOT 6572 should be issued to read the input data into AC0-11. (Figure 6-23).

4. The CPU should then execute IOT 6573 to clear DATA READY. This also sends a pulse out on the DATA ACCEPTED out line on the input cable. This signal should be used by the external device to negate the SET DATA READY signal.

6.11.4 Strobe

IOT 6577 (Figure 6-21) creates a pulse on the STROBE line that goes from the high to low state at TP3 of IOT 6577 and returns to the high state at the next TS1. This pulse may be used to start an event external to the CPU or it may signal the end of an event.

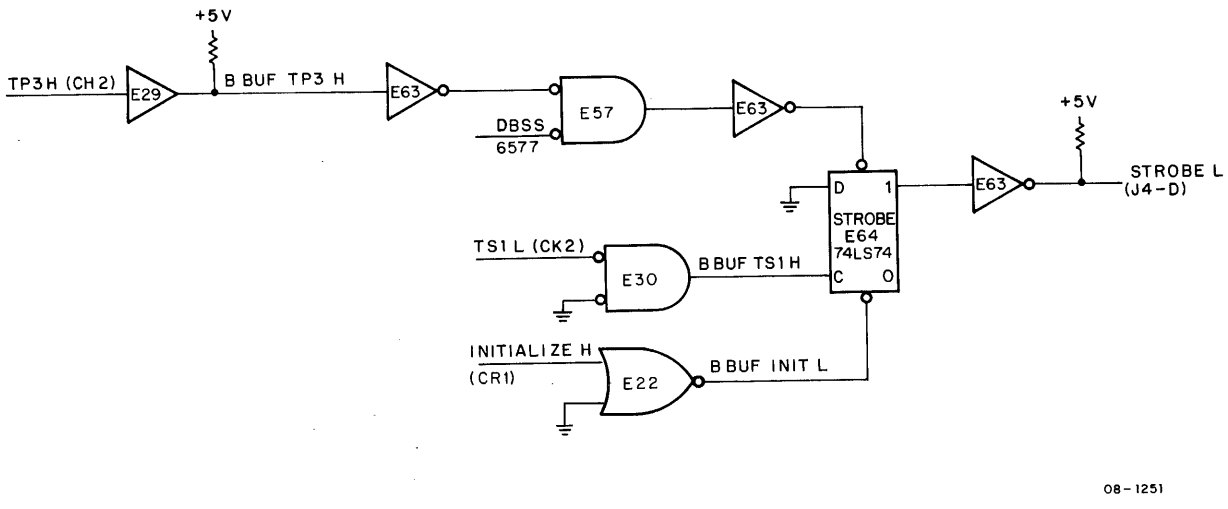

Figure 6-21 Parallel I/O Strobe Logic

6.11.5 Parallel I/O Output Register

The Parallel I/O output register (Figure 6-22) is loaded from the AC by a 6574 instruction and is loaded into the Transmit Buffer at TP3 time.

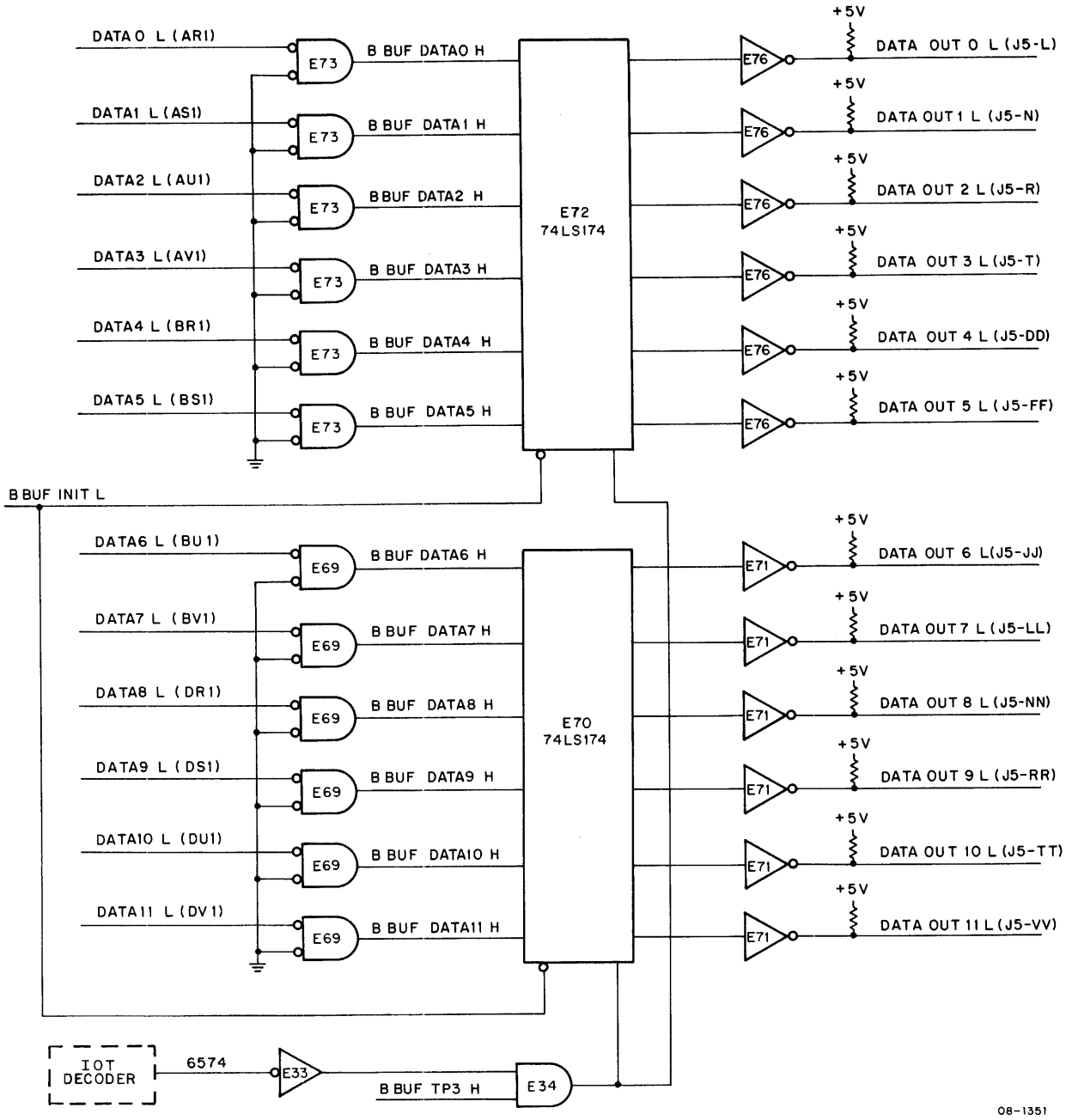

Figure 6-22 Parallel I/O Output Register

6.11.6 Parallel I/O Input Buffer and Data Gates

The information received from the device (Figure 6-23) is transferred to the AC via the Data Bus by the 6572 instruction. CO L and C1 L (Figure 6-20) are asserted (low) to allow data to be transferred from the Data Bus to the AC.

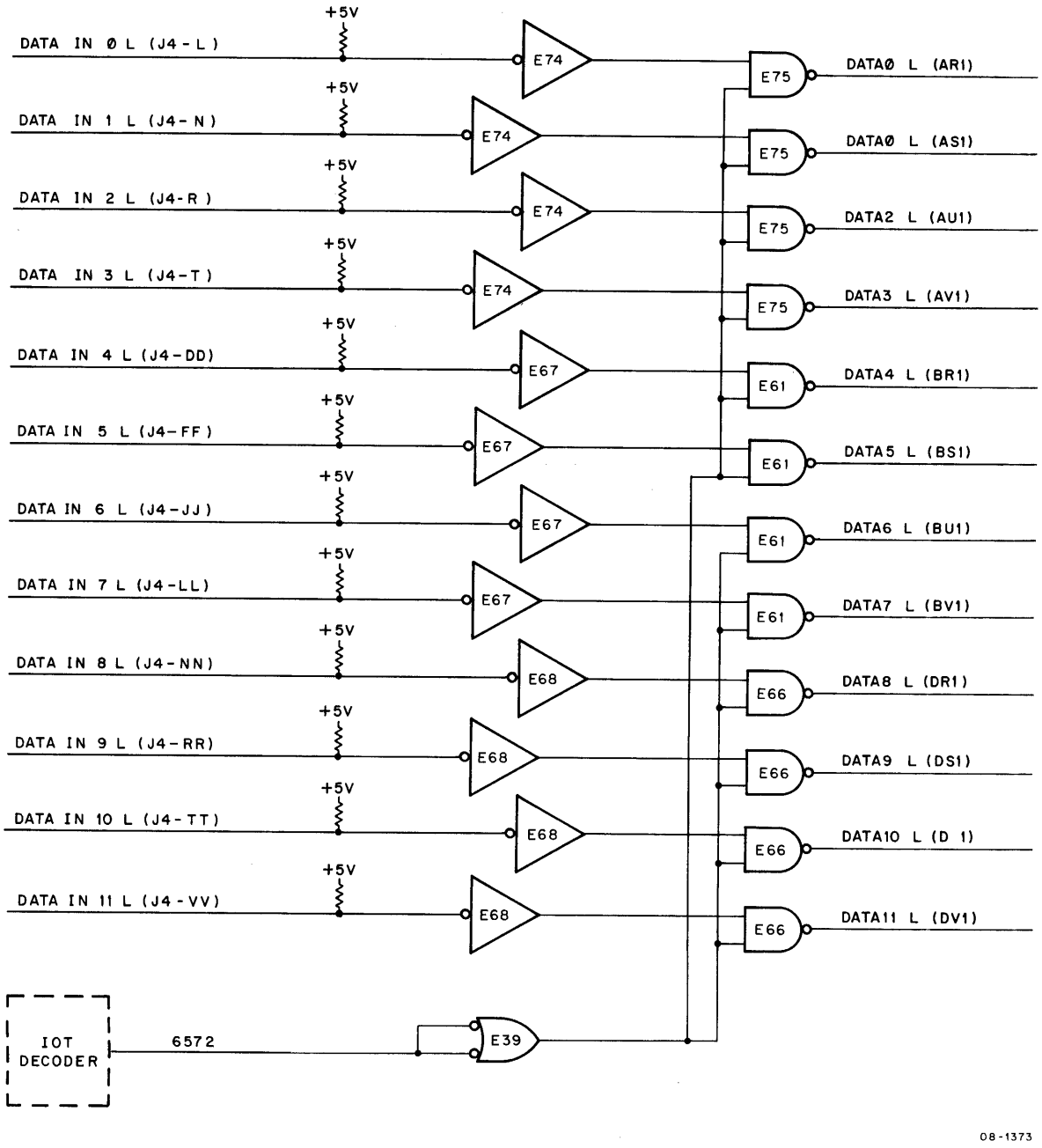

Figure 6-23 Parallel I/O Input Buffer and Data Gates