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IDENTIFICATION

PRODUCT CODE: MAINDEC-8E-D1GA-D- (D)
PRODUCT NAME: PDP-8E MEMORY POWER ON/OFF TEST
DATE CREATED: OCTOBER 28, 1970
MAINTAINER: DIAGNOSTIC GROUP
AUTHOR: BRUCE HANSEN

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1. ABSTRACT

This program is a Memory Data Validity Test to be used after a simulated power fail.

2. REQUIREMENTS

Equipment

PDP-8E equipped with Teletype

Storage

Memory locations 0000_8 - - 7601_8

Binary loader and Rim must be stored in last memory page.

3. USAGE

3.1 Loading

Normal binary tape loading procedures

3.2 Start up and/or Entry

Load address 0200 , press Clear and then cont. The program should then halt at location 0031_8 . Load address 0201 , press Clear and then Cont. The program should now loop.

3.3 Errors in Usage

Errors detected by the program cause the program to halt at memory location 0047_8 . The contents of memory address 0011_8 and 0012_8 indicate the addresses of the data that failed to check-sum. Memory addresses 0007_8 and 0010_8 contain the data words that failed to check-sum.

Lower Address = (0011_8) = 202_8 - 4001_8

U Upper Address = (0012_8) = 4002_8 - 7601_8

Lower Error Word = (0007_8) = 2525_8

Upper Error Word = (0010_8) = 5252_8

3.4 Error Recovery

Press Continue to test for other error words in memory. To reload memory do 3.2

4. DESCRIPTION

4.1 This program tests memory for bit drop out and pick up after a simulated power failure has occurred.

By starting the program at memory address 200_8 , data words consisting of 2525_8 are written into memory locations $0202_8 - - 4001_8$, and data words consisting of 5252_8 are written into memory locations $4002_8 - - 7601_8$ after which the program halts at memory address 0031_8 . Load address 0201_8 and restart the program; the program will 2's add the contents of memory location 202_8 with 4002_8 . If the results equals 7777_8 the program will 2's add the contents of memory locations 203_8 with 4003_8 etc. Until the memory addresses of 4001_8 and 7601_8 are tested. The program stays in the 2's add compare loop until an error occurs. Concurrently cycle the power to the PDP-8E off an on. After the power has been reapplied to the PDP-8E, load address 201_8 and press clear and then continue. If an error occurred during the power cycling, the program halts at location 0047_8 . The program maybe restarted at memory address 0201_8 as manytimes as desired. Restart address to fill memory with data words is 0200_8 .

4.2 Examples and/or Applications

A HALT occurs at memory address 0047_8 .

Address $0007_8 = 2535$ (Data Word)

Address $0010_8 = 5252$ (Data Word)

Address $0011_8 = 0270$ (Address Word)

Address $0012_8 = 4070$ (Address Word)

Bit 8 was picked up at memory address 0270_8 .

5. Execution Time

1 msec/loop

/PDP 8E MEMORY POWER ON OFF TEST

```

0200 0200 *200 JMP START
0201 5032 JMP COMPAR

0000 *0 0
0001 5001 JMP 1
0002 0002 2
0003 0003 3
0004 0000 0
0005 0000 0
0006 0000 0
0007 0000 0
0010 0000 UPPER, 0
0010 0000 LOWER, 0
0011 0000 LOWM, 0
0012 0000 HIGH, 0
0013 7300 START, CLA CLL /START INITIAL
0014 1056 TAD K0201
0015 3011 DCA LOWM
0016 1057 TAD K4001
0017 3012 DCA HIGH
0020 1260 WRKON, TAD UPREG
0021 3411 DCA I LOWM
0022 1061 TAD LOREG
0023 3412 DCA I HIGH
0024 1011 TAD LOWM
0025 7041 CIA
0026 1057 TAD K4001
0027 7640 SZA CLA
0030 5020 JMP WRKON
0031 7402 STEND, HLT /TURN POWER ON OFF
0032 7300 COMPAR, CLA CLL
0033 1056 TAD K0201
0034 3011 DCA LOWM
0035 1057 TAD K4001
0036 3012 DCA HIGH
0037 1411 TAD I LOWM /LOWM=UPPER ADDRESS 202-4001
0040 3007 DCA UPPER
0041 1412 TAD I HIGH /HIGH=LOWER ADDRESS 4002-7601
0042 3013 DCA LOWER
0043 1007 TAD UPPER
0044 1010 TAD LOWER
0045 7040 CMA
0046 7440 SZA
0047 7402 E1, HLT /ERROR, DOES NOT COMPARE
0050 1011 TAD LOWM
0051 7041 CIA
0052 1057 TAD K4001
0053 7640 SZA CLA
0054 5037 JMP COMPAR+5 /RETURN TO CHECK MEMORY
0055 5032 JMP COMPAR /END OF TEST AREA GO TO SETUP
0056 0201 K0201, 0201
0057 4001 K4001, 4001
0060 2525 UPREG, 2525 /ERROR WORD 2525

```

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0061 5252

LOREG,5252

/ERROR WORD 5252

\$

0000	11111111	11111111	11111111	11111111	11111111	11111111	11000000	00000000
0100	000 0000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
0200	110 0000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
0300	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

0400
0500

0600
0700

1000
1100

1200
1300

1400
1500

1600
1700

2000
2100

2200
2300

2400
2500

2600
2700

3000
3100

3200
3300

3400
3500

3600
3700

COMPAR	0032
E1	0047
HIGH	0012
K1201	0056
K4001	0057
LOREG	0061
LOWER	0017
LOWM	0011
START	0013
STEND	0031
UPPER	0007
UPREG	0060
WRKON	0020

ERRORS DETECTED: 0

LINKS GENERATED: 0

RUN-TIME: 1 SECONDS

2K CORE USED