SECTION 4 – MEMORY SYSTEM

3.22 MEMORY SYSTEM, GENERAL DESCRIPTION

The standard PDP-8/E core memory (designated MM8-E) is a random access, coincident-current, magnetic READ/WRITE core memory with cycle times of 1.2 μs and 1.4 μs. The memory comprises ferrite cores wired in a 3-D, 3-wire, planar configuration. The basic unit can store up to 4096 (4K) 12-bit words. The memory can be expanded to 32K words in 4K increments.

3.23 MEMORY SYSTEM, FUNCTIONAL DESCRIPTION

The memory system performs three basic functions for the PDP-8/E processor:

a. It decodes and selects the desired core location in which a 12-bit word is stored or will be stored.

b. It reads a 12-bit word from the selected location.

c. It writes a 12-bit word into the same selected location.

These functions are illustrated in Figures 3-31 and 3-32, for which one memory cycle is represented. The processor must first supply the address (refer to Chapter 4, Section 1, Memory Addressing, of the *PDP-8/E & PDP-8/M Small Computer Handbook)* before a read or write operation can be considered. The CPMA Register (Paragraph 3.34) is loaded at TP4; the content of the CPMA is placed on the MA lines. Memory address decoders receive the MA bits and turn the corresponding Read current switch on when control signals RETURN, SOURCE, and WRITE L (not) are present. The Memory Register is cleared when RETURN and NOT WRITE L become active (WRITE L is high and RETURN is high).

The outputs from the 12 selected cores are fed to their respective sense amplifiers. A strobe signal is used to gate the Sense Amplifier into the local Memory Register. If MD DIR L is low (as it always is during the READ portion of the memory cycle), the output of the Memory Register is placed on the MD lines. During the WRITE portion of the memory cycle, the memory selection system uses the same address inputs and control signals; however, control signal WRITE L will change states, causing the write current switches to be activated. To write the content of the Memory Register back into core, MD DIR L will be low (active). Otherwise, the content of the MB Register will be placed on the MD lines, and the word in the MB Register will be written into core. The INHIBIT L signal controls the gating circuits, and only when INHIBIT L is active will the Inhibit Drivers be activated. A 0 received from the MD lines and INHIBIT L causes the corresponding Inhibit Driver to produce inhibit current.

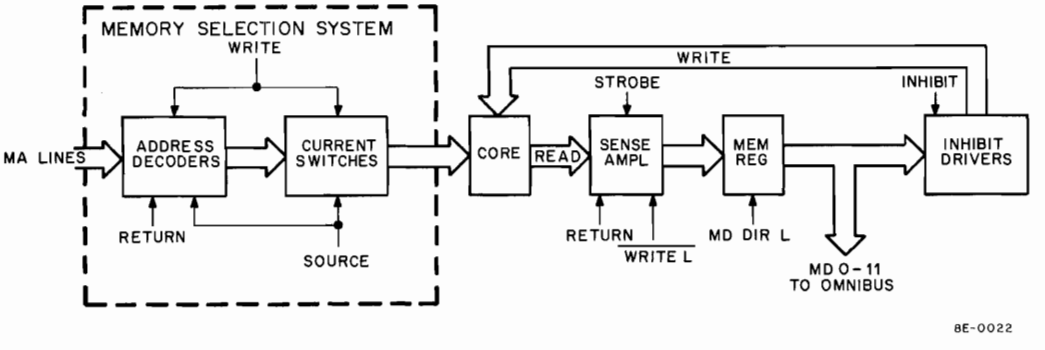


Figure 3-31 Memory System Functional Flow Diagram

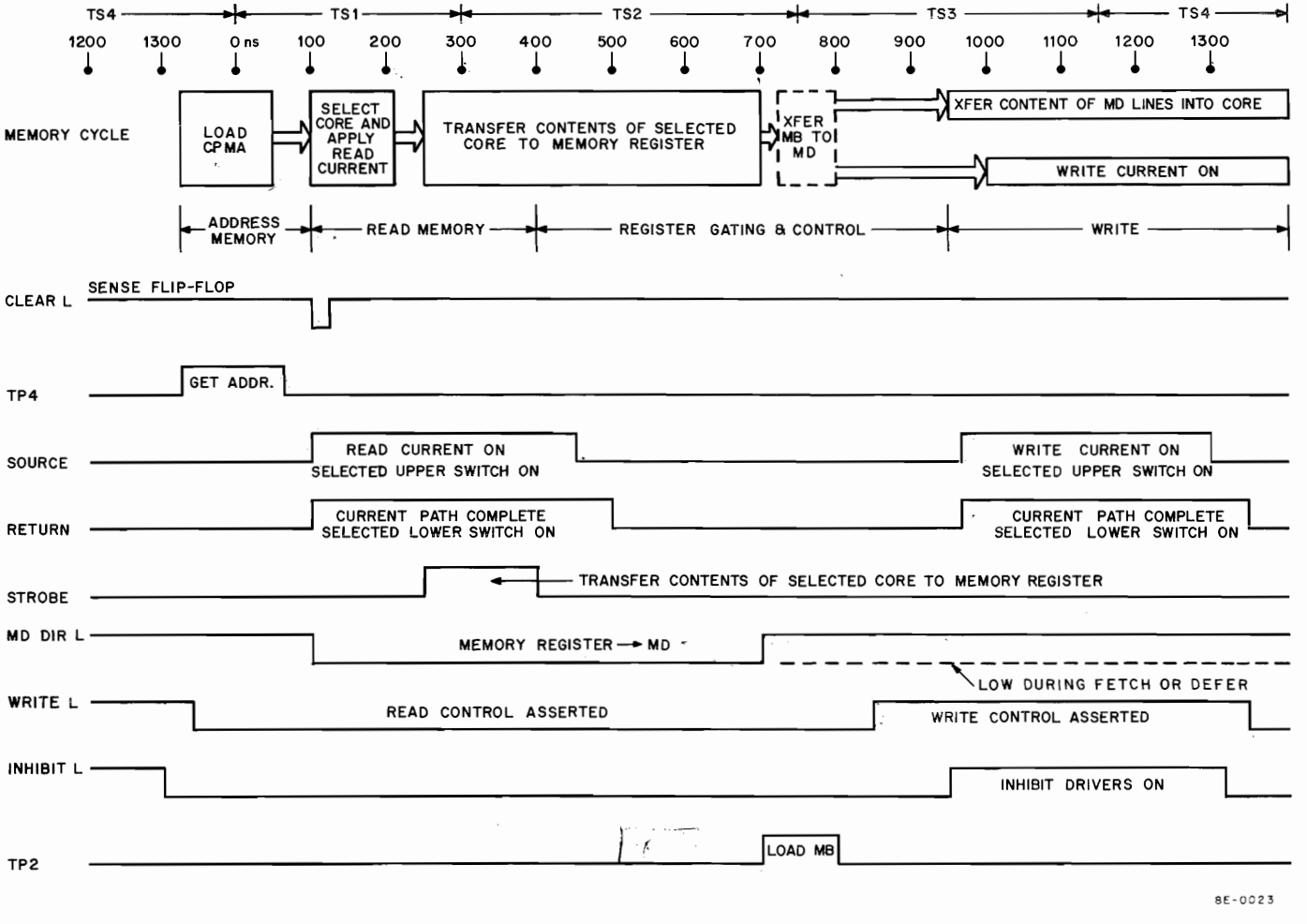


Figure 3-32 Memory Cycle Timing

3.24 MEMORY SYSTEM, DETAILED THEORY

The organization of the memory system is illustrated in Figure 3-33. Three quad-size boards are used to contain the memory system as follows:

a. G104 Sense/Inhibit contains 12 Sense Amplifiers, Memory Registers, and Inhibit Drivers with the corresponding control logic, slice control, -6V supply and current control;

b. G619 Memory Stack contains 12 mats of 4096 cores per mat, and X/Y diode selection matrix;

c. X/Y Driver and Current Source contains address decoding and selection switches, X-current source, Y-current source, and stack discharge switch-power ON/OFF protection circuit.

The detailed theory of core memory, memory selection system, and the memory sense/inhibit function is described in the following paragraphs.

3.25 CORE MEMORY

The basic storage element in the MM8-E Memory System is a small toroidal (ring-shaped) piece of magnetic material, called a magnetic core. A single core, mounted on a ground plane, is illustrated in Figure 3-34. Three wires pass through each core to accommodate the X- and Y-selection and the sense/inhibit function. A primary difference between the PDP-8/E and its predecessors is the combination of the SENSE line with the INHIBIT line to form a three-wire system instead of a four-wire system.

3.25.1 Hysteresis Loop

The characteristics of the magnetic core can be shown by a graph, plotting the current (the magnetizing force) versus flux-density (the resulting magnetism) hysteresis loop as illustrated in Figure 3-35. This hysteresis loop illustrates the magnetizing current, I, produced by the current contained in the three wires plotted along the horizontal axis, and the resulting flux density, B, through the core along the vertical axis. Two directions of current are shown. READ current, with respect to the graph, is directed from right to left. If a logic 1 is stored in the core, B will move from the remanent point ($+B_r$) down to saturation at $-B_m$ when the READ current is turned on. When the magnetizing current is removed, the flux density settles down to the remanent point at $-B_r$. WRITE current is directed from left to right with respect to the graph. If a 1 is to be written into core, the flux density will move the point $-B_r$ to point $+B_m$ on the graph and then settle down to $+B_r$ when the magnetizing current is removed. Thus, points $-B_m$ and $+B_m$ are the extreme saturation points, and points $-B_r$ and $+B_r$ are the extreme points in the normal logic states.

3.25.2 X/Y Select Lines

Core saturation occurs only when both the X- and Y-select lines each contain half the amount of current required to reach saturation. This is called the coincident current technique and results in a fully selected core. If either X- or Y-line contains no current, there is no significant change in flux density. For example, for a READ, if the core is in logic 1 state, the flux change is from point $+B_r$ to H on the graph and then reverts back to point $+B_r$. For a WRITE, the flux change is from point $-B_r$ to point J and then reverts back to $-B_r$.

3.25.3 READ Operation

READ occurs during the first half of the memory cycle. Its function is to sample either a logic 1 or logic 0 in a fully selected core. Thus, both the X- and Y-Read half-select currents must be applied for the Sense/Inhibit line to receive a pulse resulting from a change in flux density if the core is in the logic 1 state. If the core is in the logic 0 state, no change in flux density occurs and, therefore, no pulse appears on the Sense/Inhibit line.

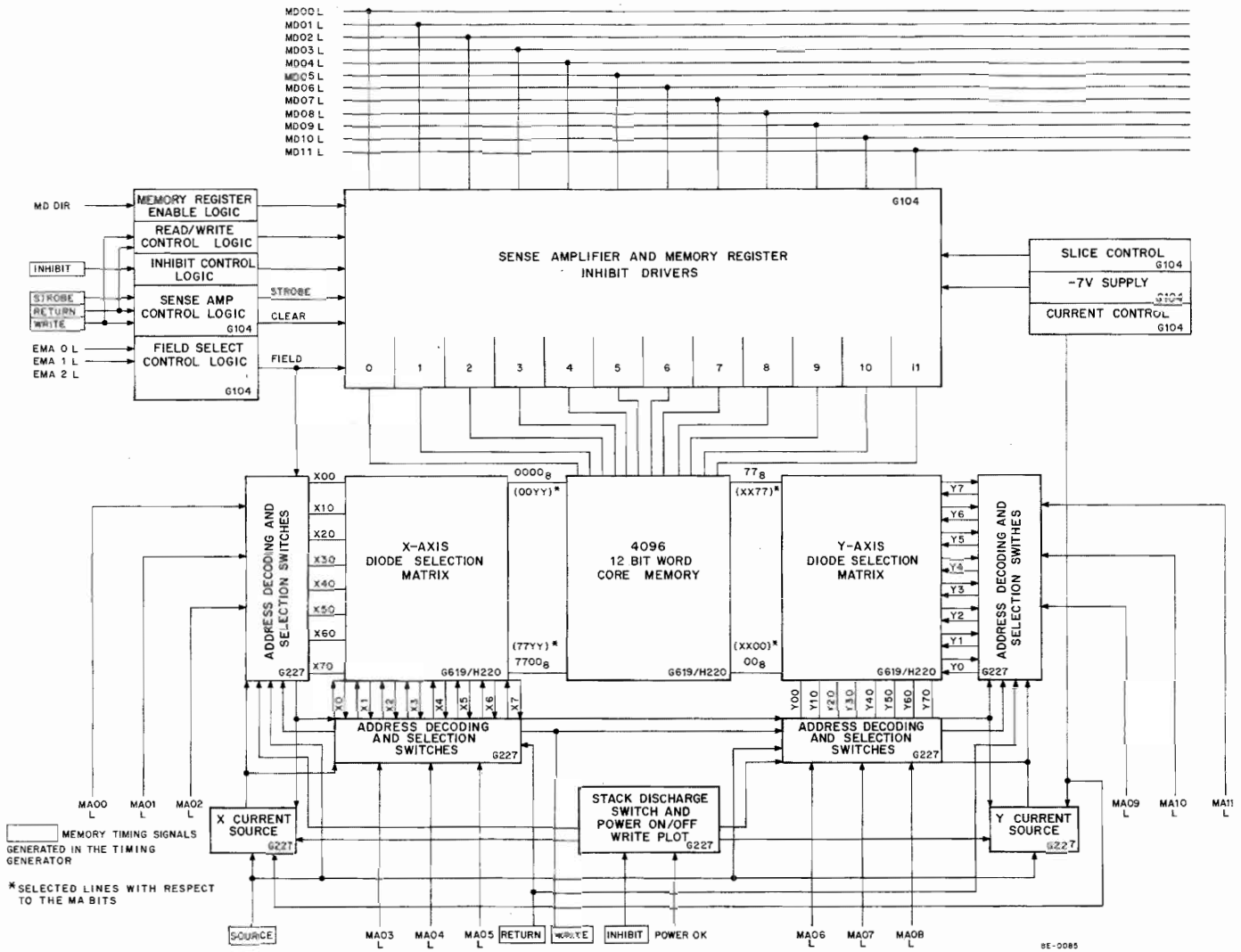


Figure 3-33 Memory System Block Diagram

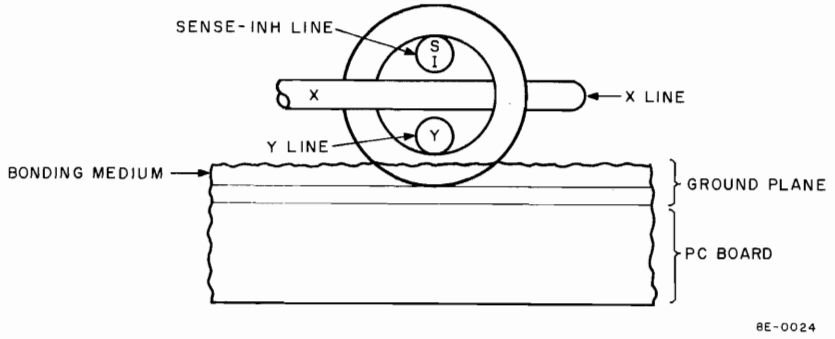


Figure 3-34 Magnetic Core

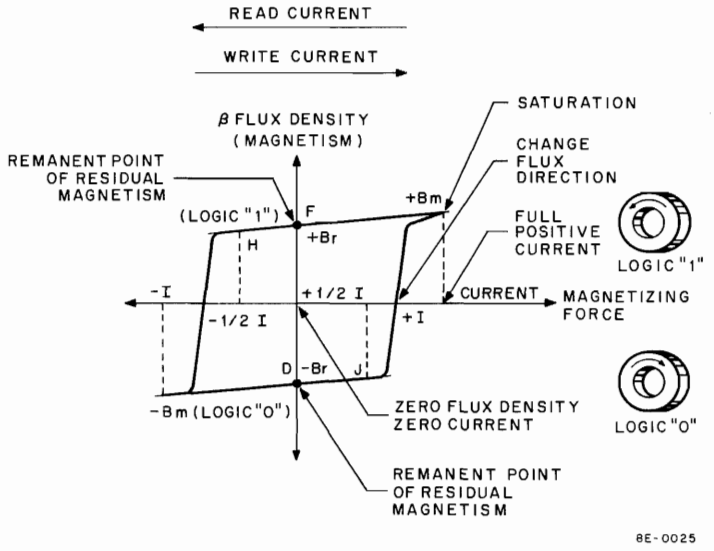


Figure 3-35 Magnetic Core Hysteresis Loop

3.25.4 WRITE Operation

WRITE occurs during the second half of the memory cycle. Because WRITE follows READ, the cores at the selected address have been cleared to a logic 0 state. If the fully selected core (X- and Y-currents) is not inhibited, the magnetic flux moves from point $-B_r$ to $+B_r$ on the graph, and a 1 is stored in core. However, to store a 0 in core, it is necessary to cause a less than fully selected condition. This can be achieved by generating an inhibit current and applying this current to the Sense/Inhibit line. If this inhibit current is in the opposite direction to the X- and Y-current, the net result of the change in flux will be from point $-B_r$ to point J on the graph. When all currents are removed, the flux density reverts back to $-B_r$ on the graph.

3.25.5 Magnetic Core In Two-Dimensional Array

A partial three-wire memory configuration is illustrated in Figure 3-36. Half-select currents are produced for one X-line and one Y-line. If, for example, the core at X3, Y2 is selected, the corresponding wires going through each row would contain half-select current. For the X3 row, X3, Y1 core would contain only half-select current, and X3, Y2 core would contain full-select current. All other cores in row Y2 would contain half-select current. The Sense/Inhibit line terminates at the Sense Amplifier and the Inhibit Driver in the manner shown in Figure 3-36. There are two termination points on the Sense Amplifier side, and one termination point at the Inhibit Drivers.

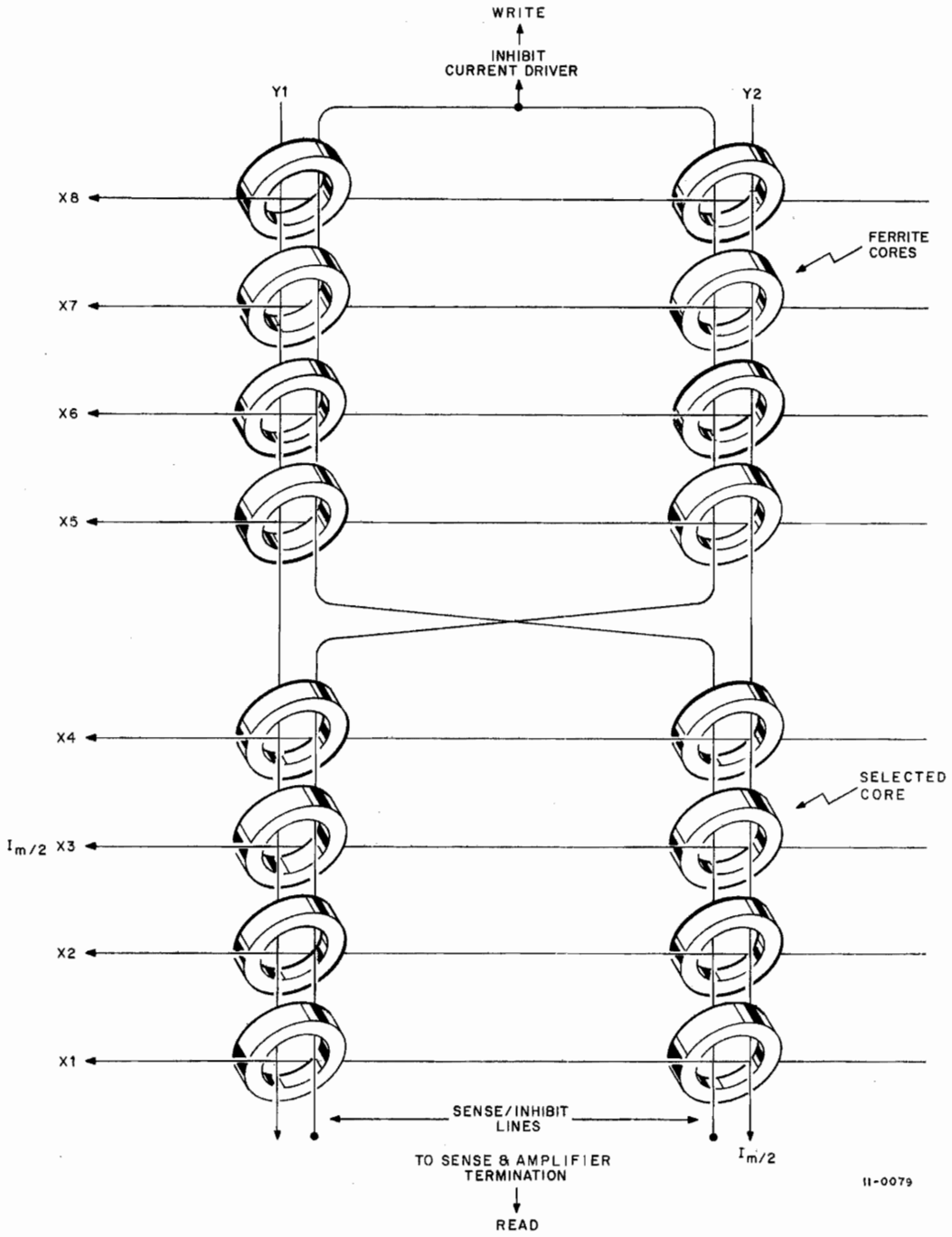


Figure 3-36 Three-Wire Memory Configuration

The third wire (the Sense/Inhibit line) receives the resulting signal at the coincident-current points during READ. Current direction is from the top of the illustration down to the Sense Amplifier. For WRITE, current direction is from the bottom of the illustration to the top to the Inhibit Current Driver. This direction opposes the current in the Y-selection line and, therefore, causes a half-select condition. This half-select procedure is only required where a 0 is to be written into core.

3.25.6 Assembly of 12-Stacked Core Mats

The MM8-E Memory is a 64 X 64 configuration (64 X-rows and 64 Y-rows). This configuration provides 4096 cores per mat, for which one core can be selected during any one memory cycle and, therefore, one bit of information per mat.

The MM8-E is a 12-bit word memory system; thus, 12 mats are used. Each mat stores one unique bit of information, which is deposited and sensed by one unique line called the Sense/Inhibit line. Thus, 12 Sense/Inhibit lines are used to deposit and sense 12 unique bits of information. The arrangement of the selection lines is quite different. All 12 mats contain 64 X-lines and 64 Y-lines. The threading of each of the X- and Y-lines continues from one mat to the next through all 12 mats. For example, row X31 of mat 0 is common to row X31 of mat 1, which is common to all subsequent mats at row X31. The common factor to each mat is the selection line that is threaded through 12 X 64 cores or 768 cores. The intersection of X31 and Y29, therefore, occurs 12 times in the 12 mats. Because each mat contains a unique Sense/Inhibit line, 12 unique bits of information can be stored to form a 12-bit word.

3.25.7 Physical Orientation of Core Memory

The memory stack layout is illustrated in Figure 3-37. Figure 3-38 illustrates the X- and Y-windings within the memory stacks.

3.26 CORE SELECTION SYSTEM

Core selection is accomplished by enabling the desired X-line and the desired Y-line and allowing current to pass through the selected lines. To accomplish the selection of the X- and Y-lines, a decoding network that receives the MA bits and decodes for line selection is required. An X- and Y-current source is also required so that each line is half-selected.

A selection system functional block diagram illustrating the parts of the memory system involved in core selection is given in Figure 3-39. The primary components involved are:

a. the memory address decoder, which receives memory address bits and control signals to select (enable) the corresponding switch and driver,

b. a current source to provide the necessary select current,

c. a driver and switch to apply current to the selected row and forward-bias the selection diode,

d. one read or write diode, which becomes forward-biased by the driver and switch while all other diodes are back-biased,

e. one selected row containing 768 cores.

The driver and switch shown in Figure 3-39 are one of 16 drivers and one of 16 switches. A WRITE operation for row X13 is illustrated to show the current path.

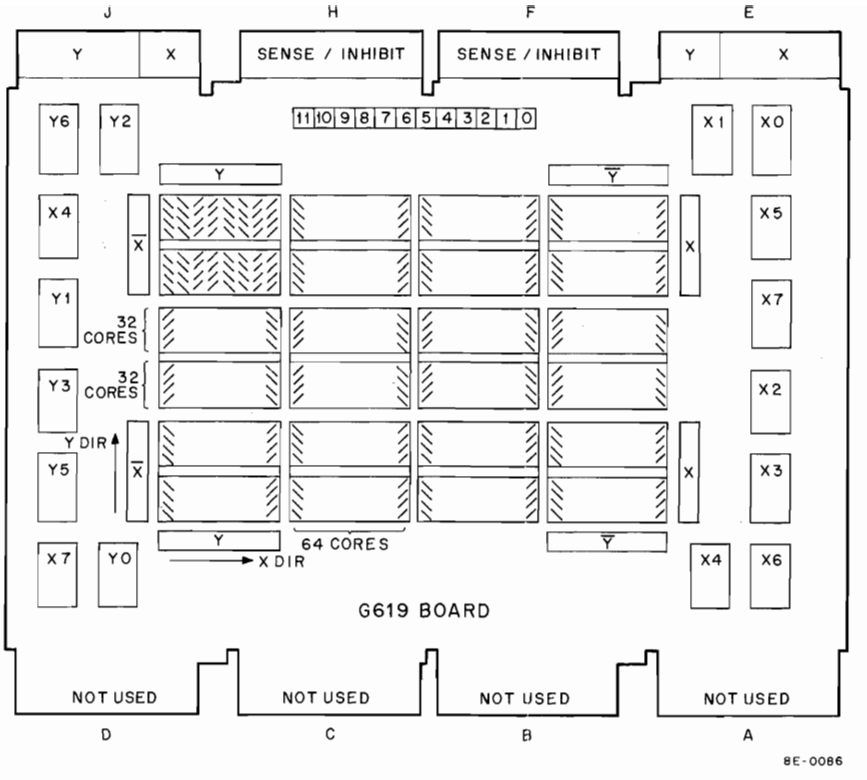


Figure 3-37 Memory Stack Layout (Core Orientation)

Both the READ and WRITE current paths are illustrated in Figure 3-40. Although not all of the circuitry is shown, the current path relationship between a READ and WRITE operation (Figures 3-40a and 3-40b) illustrates how the direction of current for WRITE is opposite to the direction for READ. The illustration also shows how the unselected components are interconnected but passive.

NOTE

Electron current flow is presented in this manual. The reader should consider current originating at a more negative voltage level and taking the path to a more positive voltage level. A forward-biased diode results when the current takes the direction opposite to the diode arrow.

3.26.1 Organization of X/Y Drivers and Current Source

Figure 3-41 illustrates the organization of the X/Y drivers and current source, and the primary signals required to make line selection and current switching possible. Eight decoders are used to select one of 64 X-lines and one of 64 Y-lines as determined by the content of bits MA0 through MA11 L. X-current and Y-current, provided by the X- and Y-current source, are applied to the drivers. The READ signal is applied to both the decoder control gates and the Bias Driver. When a READ operation is to be performed, the selected READ switches and drivers are enabled and the READ/WRITE current switch changes its output signal from ground to -15V. The negated READ signal acts to enable the WRITE function in a similar manner.

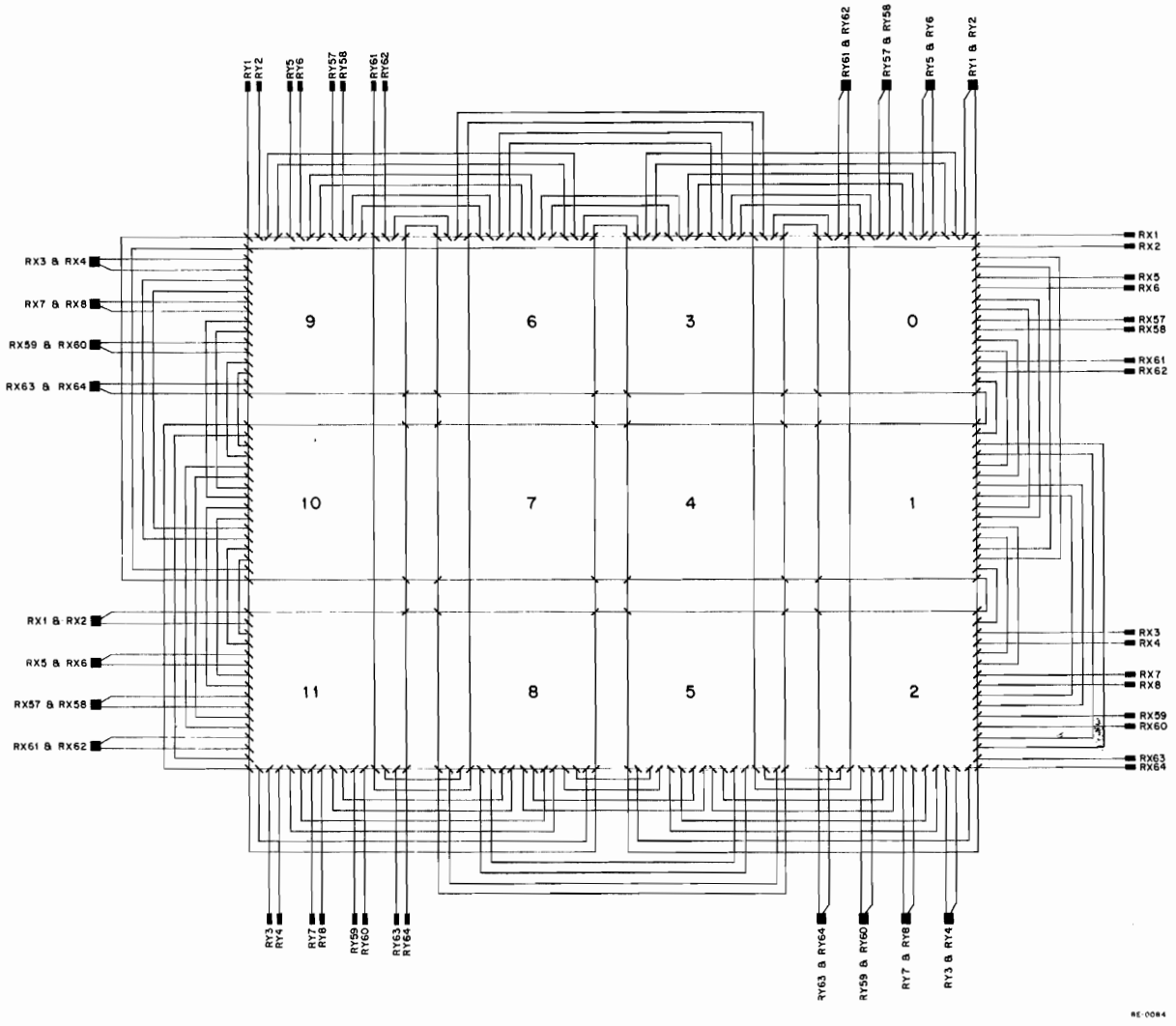


Figure 3-38 Memory Stack X, Y Windings

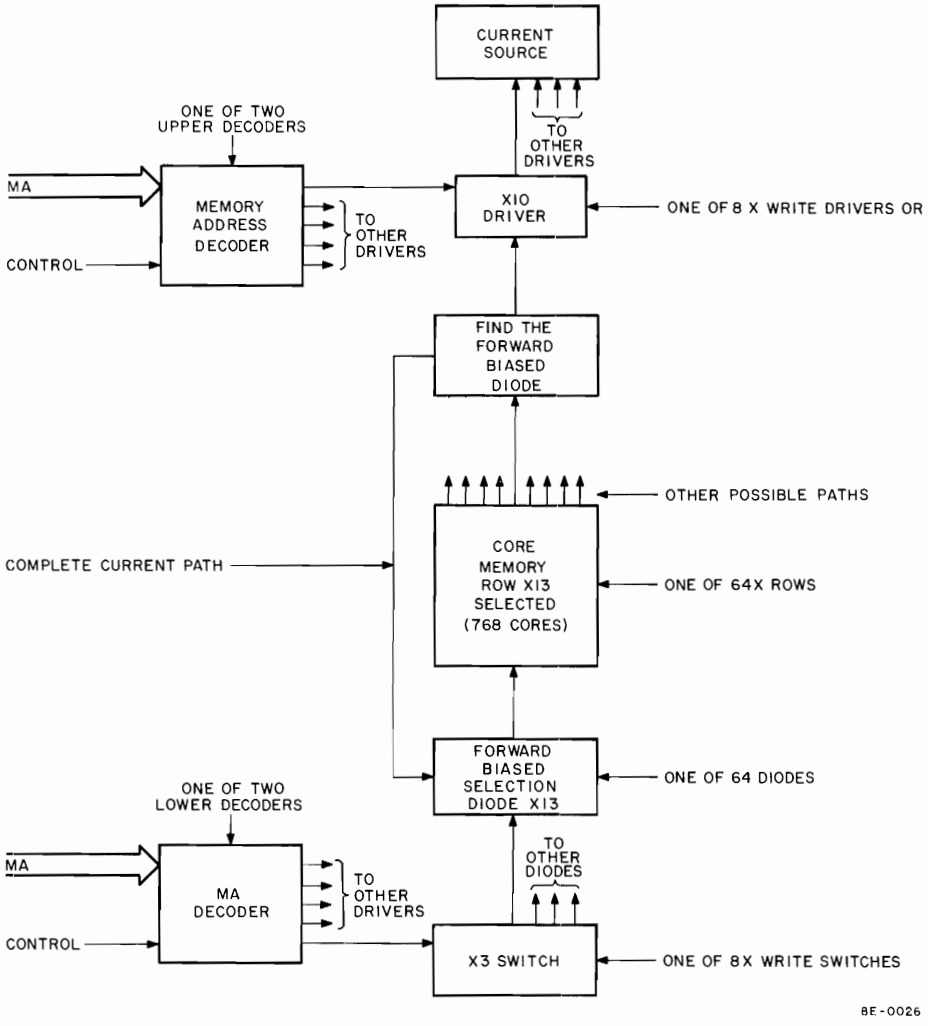
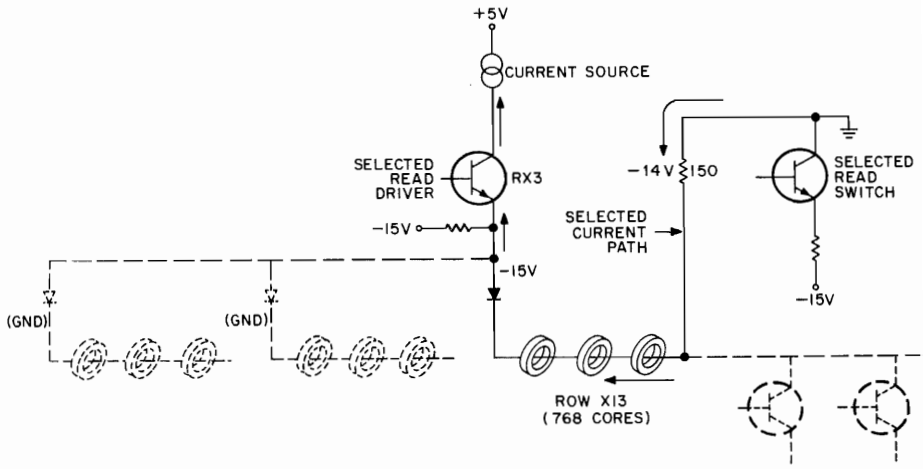
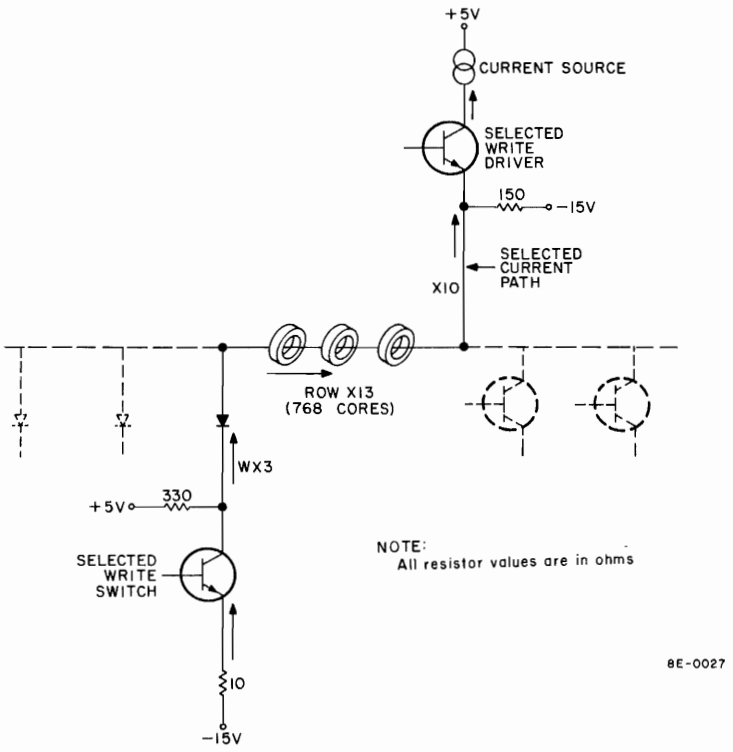


Figure 3-39 Selection System Functional Block Diagram for Write Current of X Rows



a. Current Path for Read Current



b. Current Path for Write Current

Figure 3-40 Read/Write Current Paths

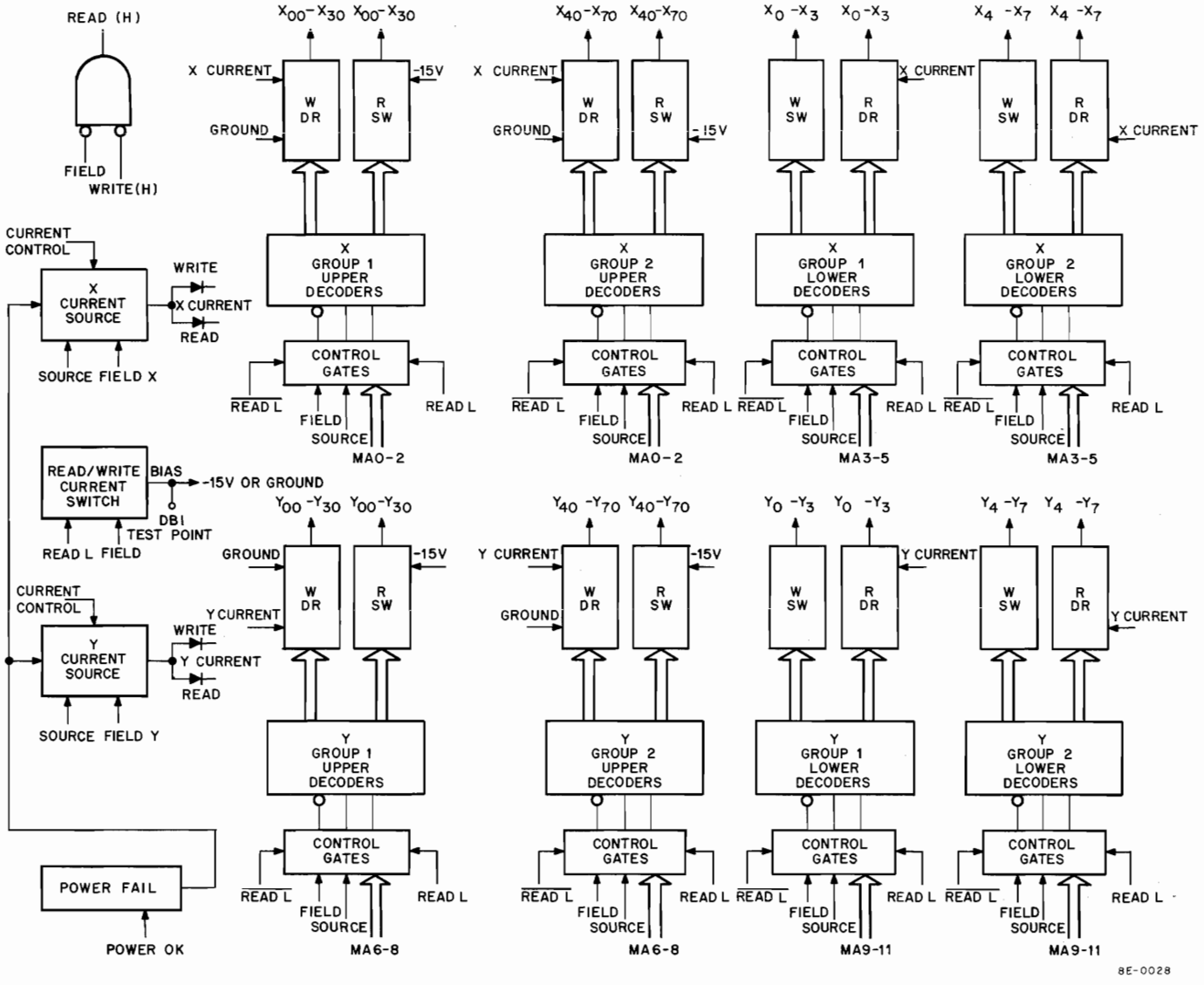


Figure 3-41 X- and Y-Drivers and Current Source
(Block Diagram Representation of G227 Circuit Schematic)

3.26.2 X- and Y-Current Sources

The X- and Y-current sources supply constant current to the READ and WRITE drivers (Figures 3-42 and 3-43). The READ and WRITE drivers receive bias voltage from the current control circuit located on the sense/inhibit board and are turned on when both FIELD and SOURCE are active. They have a slow turn-on rate and a fast turn-off characteristic due to the capacitor in the circuitry. A fast turn-off is achieved by the interaction between the capacitor and two transistors. When SOURCE is negated, one of the transistors is turned on, causing the capacitor to discharge, which causes the output transistor to be biased off. The slow turn-on time reduces the coupling effects within the core stack. Furthermore, the slow turn-on time also means that the READ current is completely controlled by the current source. Because the current source is controlled, the position of the sense output voltage relative to the drive currents is constant.

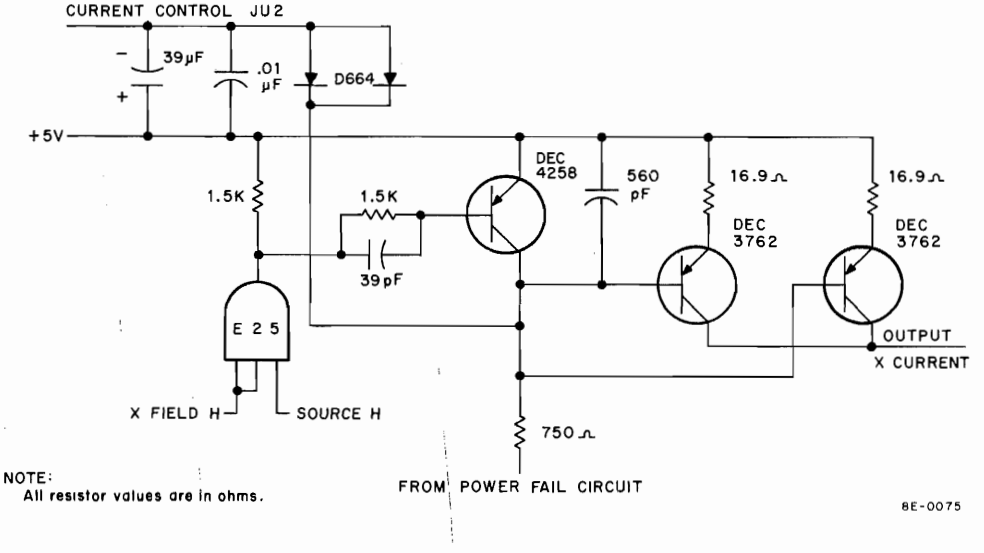


Figure 3-42 X-Current Source

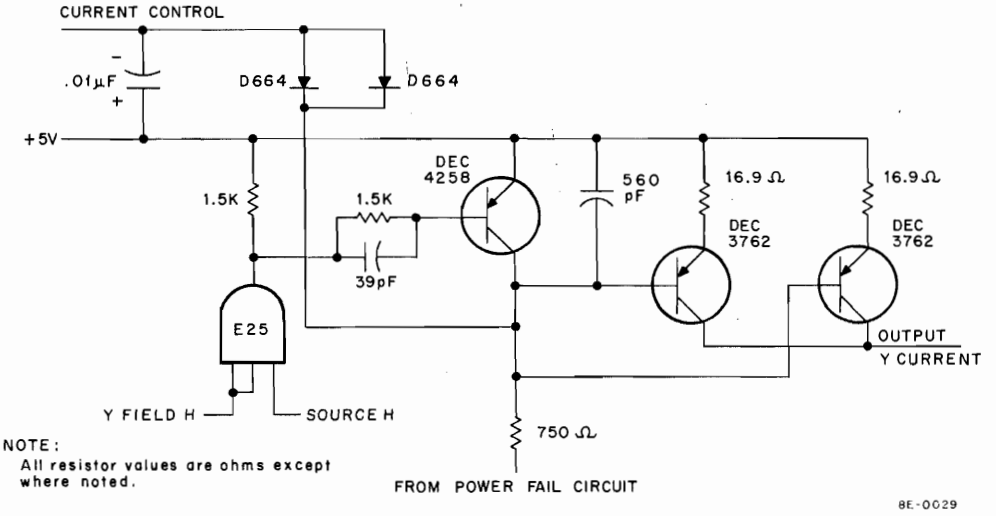


Figure 3-43 Y-Current Source

3.26.3 Bias Driver

The Bias Driver (Figure 3-44) switches the bias voltage from ground for a READ operation to -15V for a WRITE operation. When control signals READ and X FIELD are both active, level shifting circuits along with an output transistor switch the output to ground. When READ is not asserted, the output switches to -15V. The Bias Driver provides the reverse bias condition on the nonselected diodes in the memory stack. Reverse biasing the diodes reduces capacitance and, therefore, reduces "sneak currents" that might be on the line. Refer to Paragraph 3.26.7 for the organization of the planar stack diode matrix.

3.26.4 Power Fail Circuitry

The power fail circuitry (Figure 3-45) responds to the POWER OK signal from the power supply. Its primary function is to ensure that selected memory locations are not changed due to a power failure. The power supply senses a voltage change when the dc voltage drops and grounds the POWER OK line when the voltage is too low. This shuts off the timing chain but ensures that the memory cycle is completed. The memory power fail circuitry turns off the X- and Y-current source after a delay sufficient to complete the WRITE operation. When the machine is turned on initially and the POWER OK signal is asserted, the current source is activated immediately. Thus, the memory power fail circuit has a characteristic of a fast-on/slow-off switch.

3.26.5 Core Selection Decoders

Eight decoders (IC 8251) (Figure 3-41) are used to decode MA0 L through MA11 L from the Memory Address Register (refer to Appendix A for circuit description of 8251). These bits are combined with READ L, FIELD, SOURCE, and RETURN signals to enable the appropriate switch and driver. Signal READ L is generated when WRITE L is not asserted, or negated READ L results when WRITE L is active. The WRITE L signal is developed in the Timing Generator during the last half of the memory cycle. SOURCE is necessary to turn on the selected driver or switches corresponding to the upper X- and Y-select lines, and RETURN is necessary to turn on the selected drivers or switches corresponding to the lower X- and Y-select lines. Both RETURN and SOURCE are developed in the Timing Generator. RETURN remains on for 50 ns longer than SOURCE so that the lines completely discharge. FIELD is developed in the Sense Inhibit circuitry (Figure 3-47). If Extended Memory has not been addressed, this signal will be active.

3.26.6 Address Decoding Scheme

The block diagram in Figure 3-41 illustrates the method through which the MA bits are decoded; the results enable either a WRITE driver or READ switch and the corresponding driver or switch counterpart required to complete the current path. The decoder is arranged as follows: the upper select line decoders are on the left side and the lower select line decoders are on the right side of the illustration. The upper X-select line decoders decode bits MA0–2 L, while the lower X-select line decoders decode bits MA3–5 L. The upper Y-select line decoders decode bits MA6–8 L, while the lower Y-select line decoders decode bits MA9–11 L. There are a total of eight upper X-select lines, eight upper Y-select lines, eight lower X-select lines, and eight lower Y-select lines. The decoder outputs are applied to the selected switches. The outputs of the selected switches connect to the X-selection diodes (Paragraph 3.26.7) which, in turn, are connected to a line that is threaded through 768 memory cores. The arrangement of the illustration (Figure 3-41) is such that each component corresponds to the approximate location on the engineering drawing schematic (G227). This arrangement allows a quick reference to the circuits of interest.

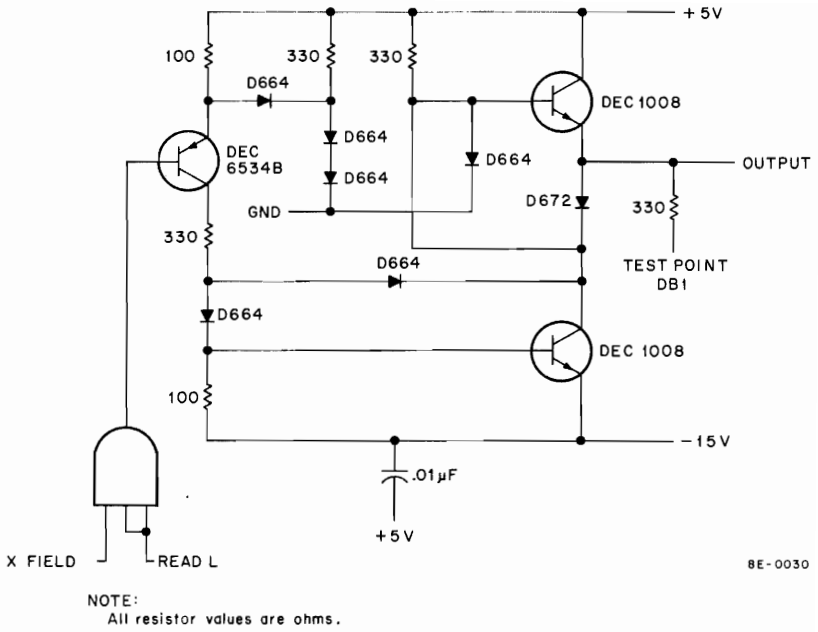


Figure 3-44 Bias Driver

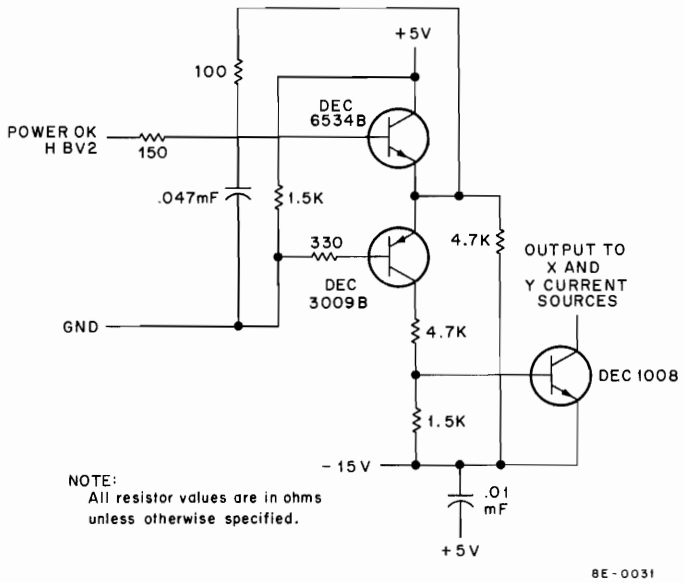


Figure 3-45 Power Fail Circuit

The decoding scheme of the MA bits is illustrated in Figure 3-46. The illustration shows the five parts of the memory address, what is decoded, and where in the field of the drawing the decoders are located. Table 3-3 lists the necessary input control signals, the content of the memory address, the input pins, the output pins, and the selected X- or Y-line. With this information, the user can easily trace through all of the components on any signal/current path to find the selected components.

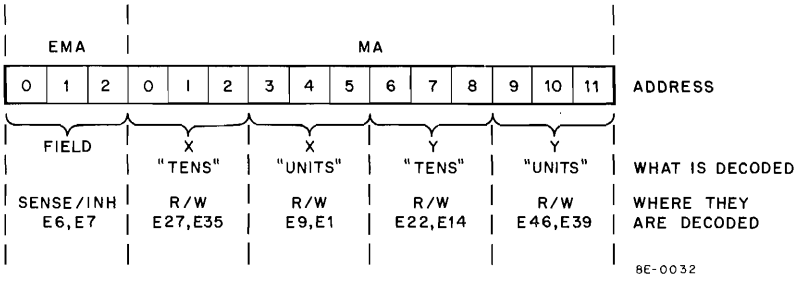


Figure 3-46 Decoding Relationships

3.26.7 Operation of Diodes

Each of the X- and Y-select lines are connected to a corresponding string of diodes (Figure 3-47). Selection is such that any one of the eight upper select lines will pass current in a path determined by whether it is a READ or WRITE operation. In the illustration given in Figure 3-47, for X-selection, the example illustrates line X_{12} being selected. The current passes through 768 cores and back through one of the diodes. The path the current takes from this point is determined by the diode that is forward-biased. The forward-biasing of a diode is accomplished by operating the switch and driver. If it is a WRITE operation, WX2 is forward-biased and the current takes the path from WX2 to X10. If it is a READ operation, RX2 is forward-biased and the current takes the path from RX10 to RX2.

NOTE

The READ and WRITE currents are opposite in direction. This is accomplished by READ L, which controls the Bias Driver circuit.

In both cases, the selection diodes are instrumental in determining the current path. All diodes except the selected diode are reverse-biased.

3.26.8 Operation of Selection Switches

Figure 3-48 illustrates the switching operation of the currents through X12 select line. On the upper side, a pair of transistors are used to either drive or switch current, depending on whether the operation is READ or WRITE. A complementary pair of transistors on the lower side are used to either drive or switch the current. Between the upper and lower side is a line that is threaded through 768 cores. The READ operation begins with the decoders. When an X-line such as X12 is to be selected, the READ driver and READ switch must first be turned on. To turn on the READ driver and READ switch, the base of each transistor must be positive with respect to the emitter. This occurs only when the output of the decoder is low (active). Otherwise, +5V is applied to the emitter side of the transformer as illustrated by S = open.

Table 3-3
Core Selection Decoding Scheme

Groups 1 and 2 – Upper X- and Y-Decoders

READ (SOURCE-)

FUNCTION	FIELD	SOURCE	WRITE L	MA 0–2 (X) MA 6–8 (Y)	Group 1 Input Pins	Group 1 Output Pins	Group 2 Input Pins	Group 2 Output Pins	Selected Line
Turn on Read Switch	L	H	L		DBA				
				000	LLL	4L	– – – – – –		X or Y 00
				001	LLH	5L	– – – – – –		X or Y 10
				010	LHL	6L	– – – – – –		X or Y 20
				011	LHH	7L	– – – – – –		X or Y 30
							DBA		
				100	– – – – – –		LLL	4L	X or Y 40
				101	– – – – – –		LLH	5L	X or Y 50
				110	– – – – – –		LHL	6L	X or Y 60
	L	H	L	111	– – – – – –		LHH	7L	X or Y 70

Table 3-3 (Cont)
Core Selection Decoding Scheme

Groups 1 and 2 – Upper X- and Y-Decoders

WRITE (SOURCE-)

FUNCTION	FIELD	SOURCE	WRITE L	MA3–5 L MA9–11 L	Group 1 Input Pins	Group 1 Output Pins	Group 2 Input Pins	Group 2 Output Pins	Selected Line
Turn on Write Switch	L	H	H		DBA				
				000	LLL	0L	– – – – – –		WX0 or WY0
				001	LLH	1L	– – – – – –		WX1 or WY1
				010	LHL	2L	– – – – – –		WX2 or WY2
				011	LHH	3L	– – – – – –		WX3 or WY3
							DBA		
				100	– – – – – –		LLL	0L	WX4 or WY4
				101	– – – – – –		LLH	1L	WX5 or WY5
				110	– – – – – –		LHL	2L	WX6 or WY6
	L	H	H	111	– – – – – –		LHH	3L	WX7 or WY7

Table 3-3 (Cont)
Core Selection Decoding Scheme

Groups 1 and 2 – Upper X- and Y-Decoders

WRITE
(RETURN+)

FUNCTION	FIELD	SOURCE	WRITE L	MA0–2 L MA6–8 L	Group 1		Group 2		Selected Line
					Input Pins	Output Pins	Input Pins	Output Pins	
	L	H	H		DBA				
Turn	↑	↑	↑	000	LLL	0L	– – – – – –		X or Y 00
on				001	LLH	1L	– – – – – –		X or Y 10
Write				010	LHL	2L	– – – – – –		X or Y 20
Drivers				011	LHH	3L	– – – – – –		X or Y 30
							DBA		
				100	– – – – – –		LLL	0L	X or Y 40
				101	– – – – – –		LLH	1L	X or Y 50
				110	– – – – – –		LHL	2L	X or Y 60
	L	H	H						
				111	– – – – – –		LHH	3L	X or Y 70

Table 3-3 (Cont)
Core Selection Decoding Scheme

Groups 1 and 2 – Upper X- and Y-Decoders

READ
(RETURN+)

FUNCTION	FIELD	SOURCE	WRITE L	MA3–5 L MA9–11 L	Group 1		Group 2		Selected Line
					Input Pins	Output Pins	Input Pins	Output Pins	
	L	H	L		DBA				
Turn	↑	↑	↑	000	LLL	4L	– – – – – –		RX 0 or RY 0
on				001	LLH	5L	– – – – – –		RX 1 or RY 1
Read				010	LHL	6L	– – – – – –		RX 2 or RY 2
Drivers				011	LHH	7L	– – – – – –		RX 3 or RY 3
							DBA		
				100	– – – – – –		LLL	4L	RX 4 or RY 4
				101	– – – – – –		LLH	5L	RX 5 or RY 5
				110	– – – – – –		LHL	6L	RX 6 or RY 6
				111	– – – – – –		LHL	7L	RX 7 or RY 7
	L	H	L						

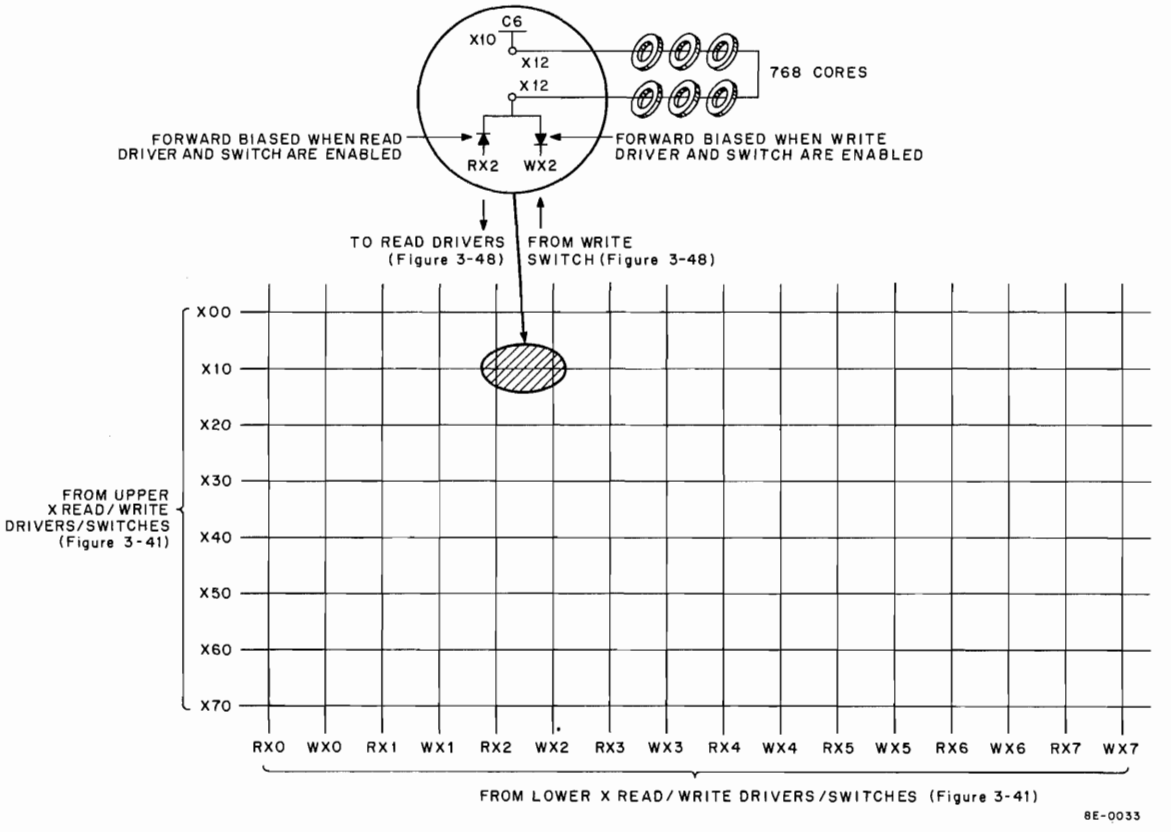


Figure 3-47 Organization of Planar Stack Diode Matrix for X Select Lines

When the READ driver is off, the +5V causes the READ diode at the current source to be reverse-biased. As soon as the READ driver is turned on, the READ diode immediately becomes forward-biased, allowing regulated current to be applied to the READ driver. The driver serves as a high-gain current amplifier, which supplies the required current to half-select any given core. A second requirement to pass READ current through core is to forward-bias the READ diode in the diode matrix. Current then passes through the READ driver, through the READ diode, through 768 cores, and back to the READ switch.

The WRITE operation is similar to READ and begins with the decoder. To select line X12, the decoder causes the WRITE driver transformer to reverse polarity, which then turns on the WRITE driver. The WRITE diode at the current source becomes forward-biased and current begins flowing through the diode, the WRITE diode of the matrix, and through 768 cores.

3.26.9 Operation of the Core Selection System

The cores that contain a selected X-line and selected Y-line define the location for which a 1 or 0 will be either written in or read out. Figure 3-49 illustrates a small portion of memory and the corresponding selection devices. Using Table 3-3, the selection of any given core can be traced from the Memory Address Register, through the decoders and switches, to the selected core.

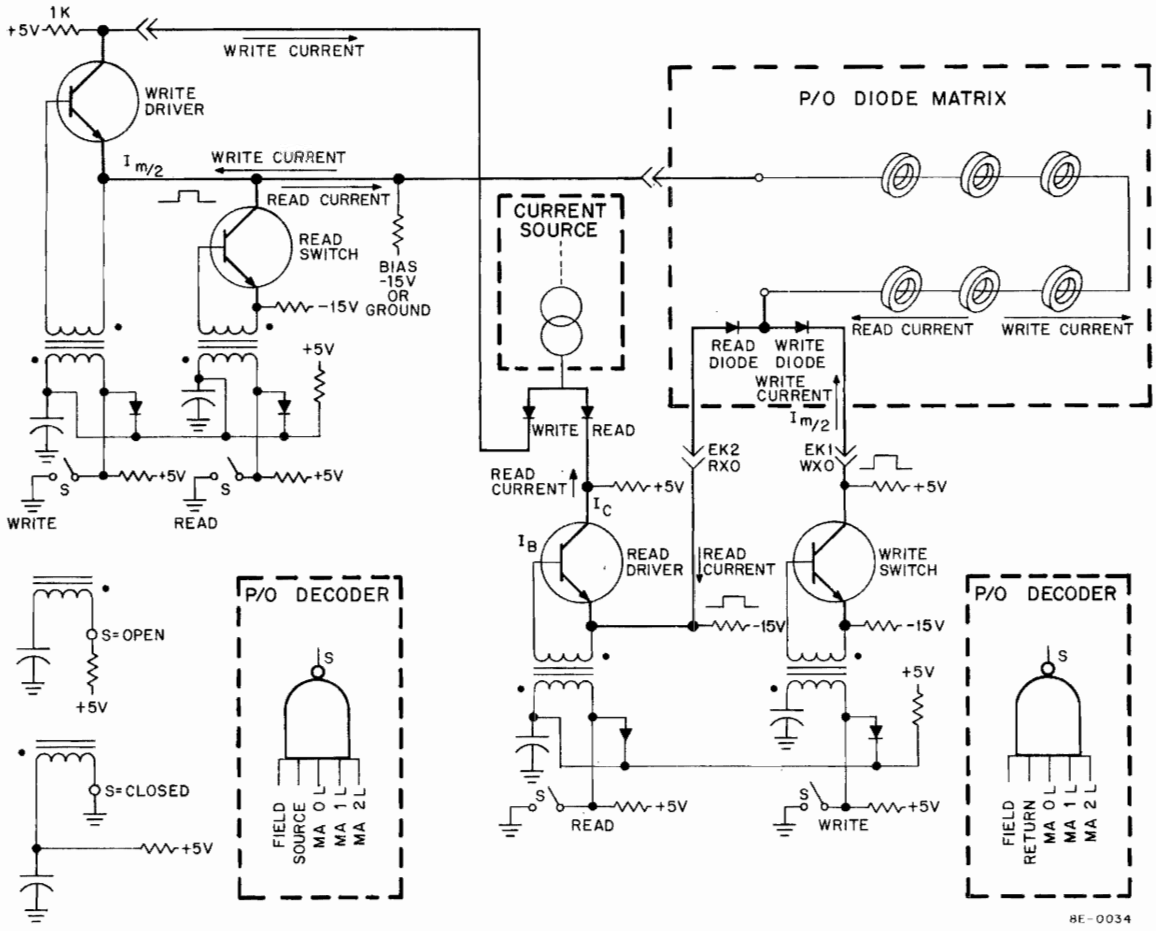


Figure 3-48 Operation of Selection Switches

3.27 SENSE/INHIBIT FUNCTION

The previous paragraphs have described the memory core, the selection of memory core, and the selection of memory core in terms of the READ/WRITE operation. However, to perform a READ or a WRITE operation, sense amplifiers are necessary to sense the state of the selected cores, and Inhibit Drivers are necessary to write 0s into core. Control logic and data registers are also required to control the data flow to and from memory. These necessary circuits are illustrated in a simplified diagram (Figure 3-50). The circuitry corresponding to the READ operation is shown on the lower portion of the illustration; the circuitry corresponding to the WRITE operation is illustrated in the upper portion of the illustration.

3.27.1 Sense/Inhibit Line

The line that is used to sense a 1 during READ is used to transmit current when a 0 is to be written during the WRITE portion of the memory cycle. The Sense/Inhibit line passes through 4096 cores of a corresponding mat. Both ends of this line are terminated at the input to the Sense Amplifier; a terminal connection is made so that the Inhibit Driver output joins this same line.

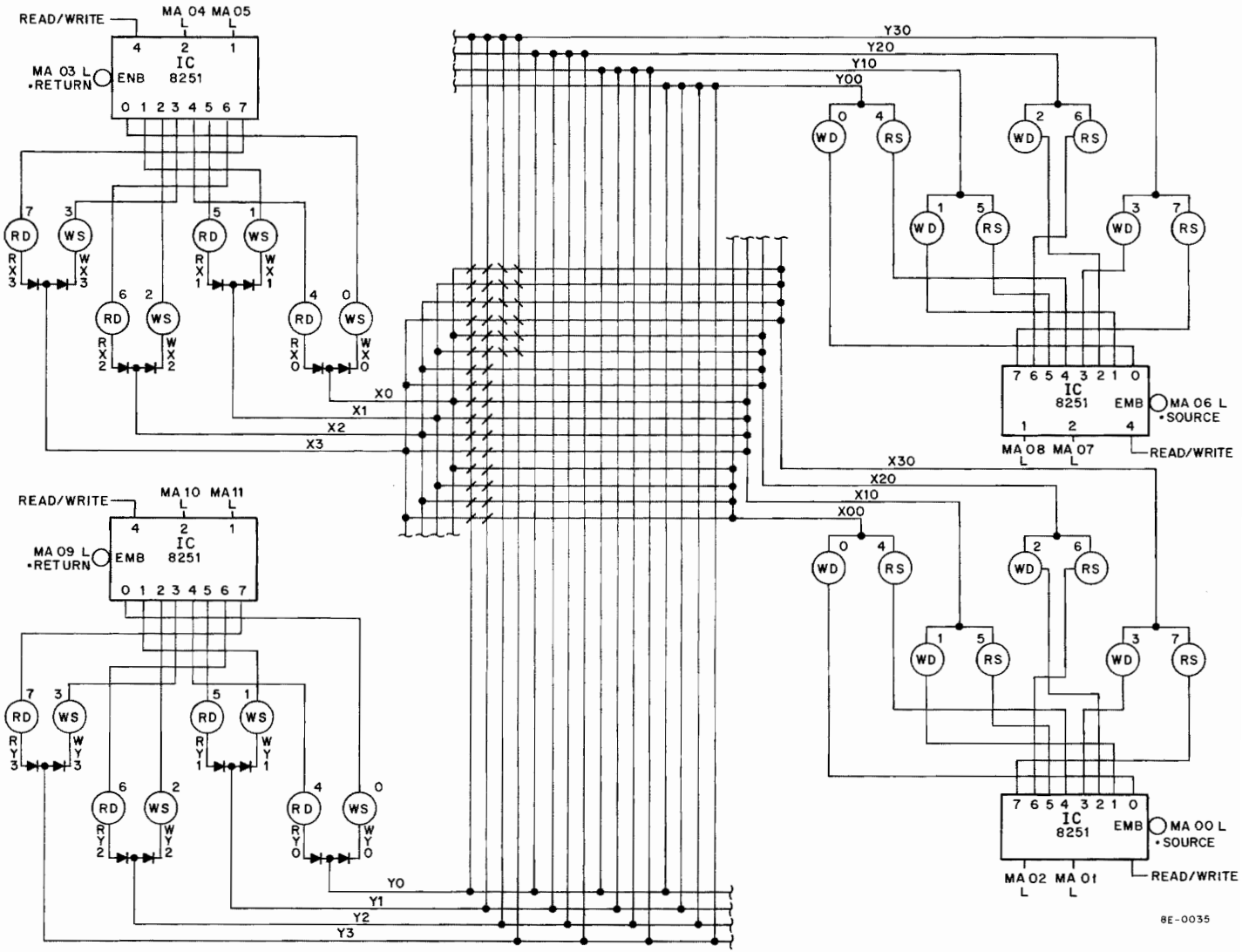


Figure 3-49 Operation of X/Y Selection Switches

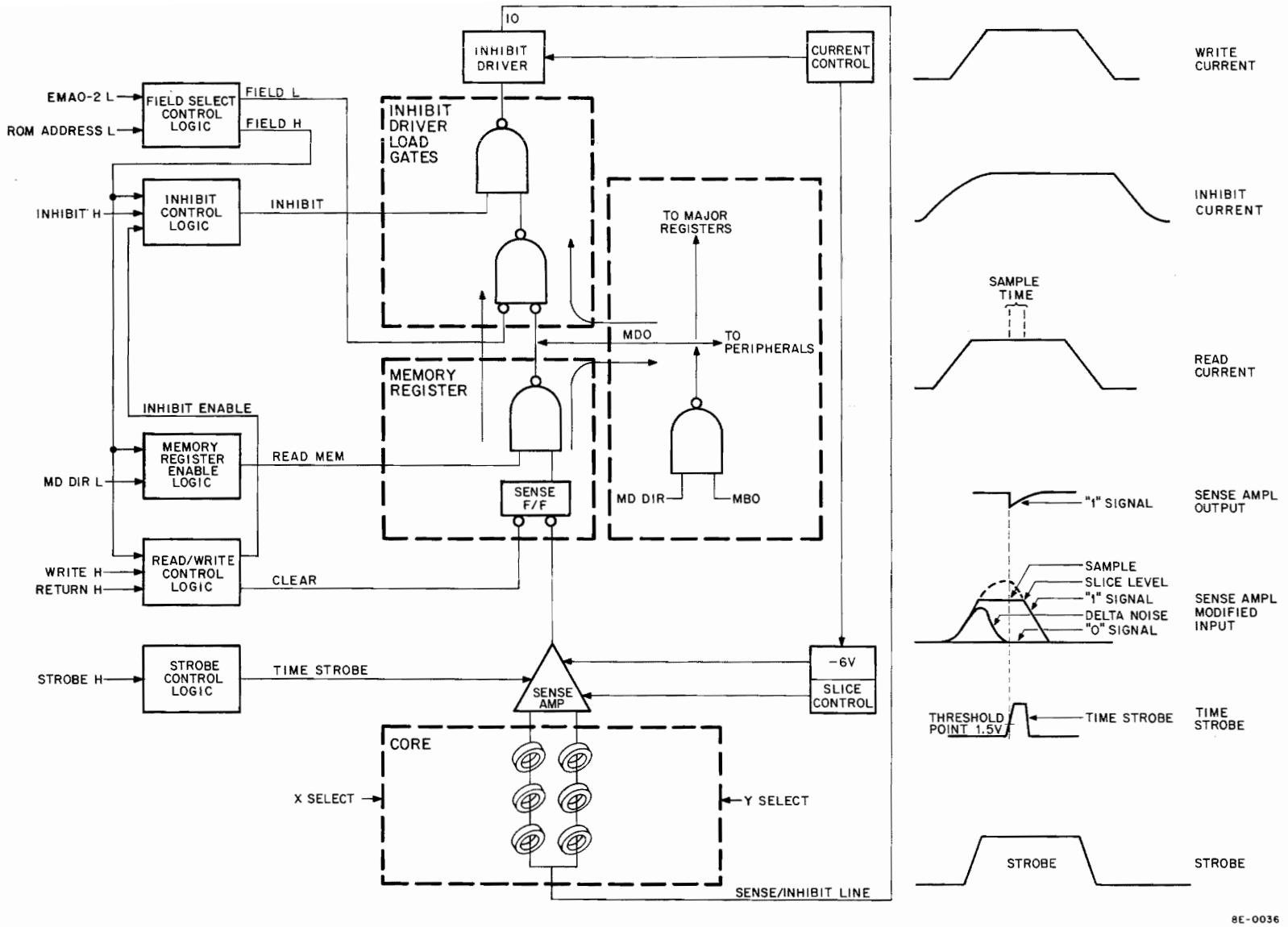


Figure 3-50 READ/WRITE Operation, Simplified Diagram (Bit 0)

3.27.2 READ Operation

The READ operation involves the Sense Amplifier, Memory Register, and the necessary control logic in conjunction with the selection system. During the READ portion of the memory cycle, the selected core develops a signal on the Sense/Inhibit line only if a 1 was previously stored in core. The SENSE flip-flops are cleared and TIME STROBE gates either a 1 or 0 out of the Sense Amplifiers and applies a corresponding pulse (if it is a 1) to the Memory Register. When a 1 is sensed, the Sense Amplifier applies a negative-going pulse to the SENSE flip-flop. The Memory Register output gate receives the SENSE flip-flop signal and gates the 1 or 0 out to the MD line. Note that the Memory Register outputs are gated onto the MD lines only when MD DIR L is low; consequently, the only requirement to write the contents of the Memory Register back into memory is to keep MD DIR L low during the WRITE portion of the memory cycle. The output of the Memory Register can be applied, therefore, to the inhibit circuits for a rewrite; or because the data is first applied to the MD BUS, the output of the Memory Register can be loaded into one of the major registers or a peripheral.

When the Memory Register applies data to the MD lines (Figure 3-2), the data can be loaded into any one of the Major Registers, as well as applied to the Inhibit Drivers for re-deposit into core. Conversely, the data contained in the Memory Buffer (MB) Register can be applied to the MD lines and to the Inhibit Drivers.

3.27.3 WRITE Operation

The WRITE operation involves the Inhibit Drivers, load gates, Memory Register, and the necessary control logic in conjunction with the selection system. The Inhibit Driver load gates receive 1s and 0s via the MD lines from either the MB Register in the processor or the Memory Register. Control gating signals for the Inhibit Driver load gates are:

a. FIELD, which indicates that field 0 has been selected,

b. INHIBIT from the Timing Generator. Inhibit current is generated by the Inhibit Drivers only when a 0 is to be written into core.

3.27.4 Field Select Control Logic

The field select control logic (Figure 3-51) determines if the basic memory has been selected. When field 0 is selected, the logic develops a signal, called FIELD, for gating other control logic and the Inhibit Driver load gates. The logic receives extended address memory bits EMA0 L through EMA2 L.

A comparison circuit compares the bits on the EMA lines with the EMA jumpers. If the two are equal and if ROM ADDRESS L is high, the field is selected. Bank 0 is always selected with all jumpers in. The Exclusive-OR gate provides a high output only when one input is high.

3.27.5 Inhibit Control Logic

The Inhibit Control logic (Figure 3-52) provides a gating control signal to the Inhibit Driver load gates during the WRITE portion of the memory cycle. The logic receives INHIBIT from timing, RETURN from the Timing Generator, FIELD from the Field Select Control logic, and WRITE ENABLE from the READ/WRITE control logic.

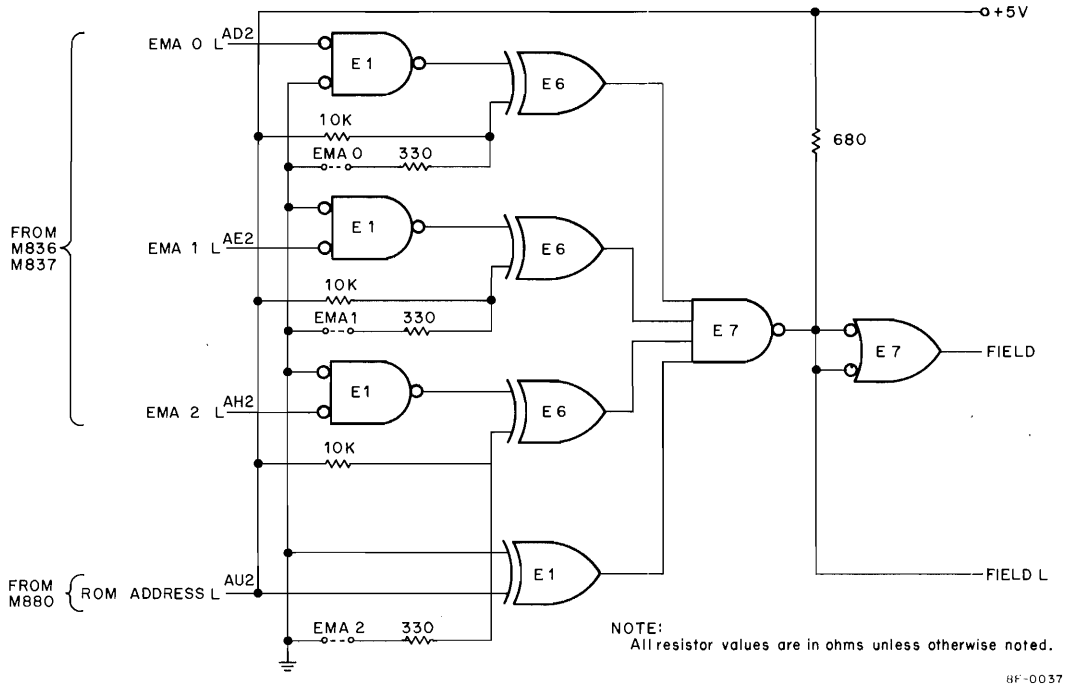


Figure 3-51 Field Select Control Logic

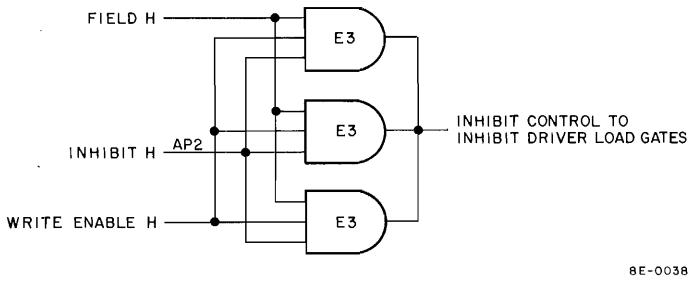


Figure 3-52 Inhibit Control Logic

3.27.6 Memory Register Enable Logic

The Memory Register Enable logic (Figure 3-53) functions when the contents of the Memory Register are to be gated onto the Inhibit Drivers and MD lines. When MD DIR L is low, the output of the control logic (READ) gates the content of the SENSE flip-flops to the MD BUS.

3.27.7 READ/WRITE Control Logic

The READ/WRITE Control logic (Figure 3-54) clears all SENSE flip-flops and enables the Inhibit Control logic.

The CLEAR L signal only becomes active when WRITE H is not active and RETURN H is asserted. This begins at the start of the READ portion of the memory cycle and continues for a period of approximately 50 ns. The CLEAR L signal becomes inactive when the E4 flip-flop is reset by the CLEAR L signal input.

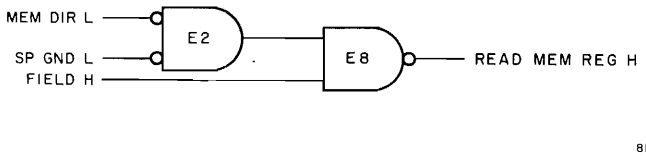


Figure 3-53 Memory Register Enable Logic

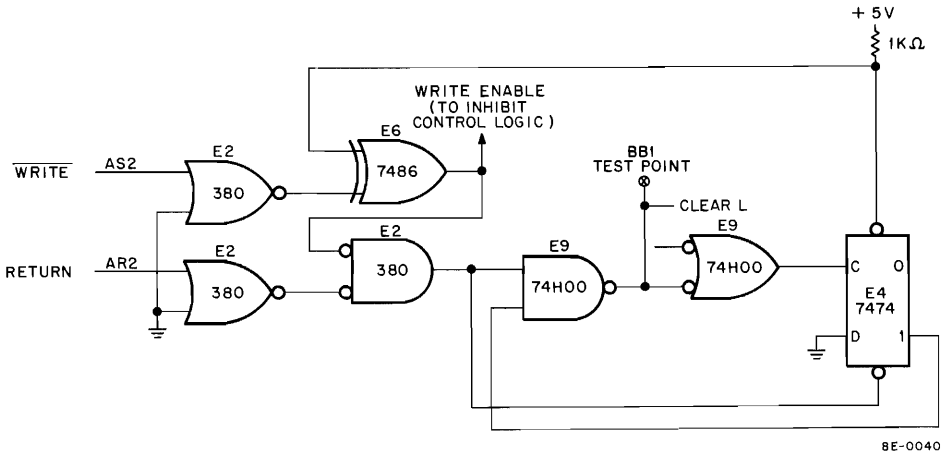


Figure 3-54 READ/WRITE Control Logic

3.27.8 Strobe Control Logic

The Strobe Control logic (Figure 3-55) is used to control the sample time of the Sense Amplifiers during the READ portion of the memory cycle. TIME STROBE occurs when WRITE L is not asserted, FIELD has been selected, and the STROBE timing signal from the Timing Generator has been received. STROBE is gated in and passed through an adjustable time-delay circuit. The flip-flop (7474) senses the rise and fall times of the strobe pulse and enables the output gate. The signal can be observed at test point CA1 (using a module extender).

3.27.9 Sense Amplifiers

Twelve Sense Amplifiers (Figure 3-56) are required to sense signals on the twelve sense lines. If the selected core in a given mat contains a 1, a pulse is received on the Sense/Inhibit winding. This pulse is amplified by the Sense Amplifier and then used to set a 1 into the Memory Register. If the selected core contains a 0, the signal received by the Sense Amplifier is small, and no pulse appears at the output of the Sense Amplifier; the Memory Register remains in the 0 state. The Sense Amplifier is "strobed" with a narrow pulse to ensure that the content of the sense lines is sampled at the proper time. This timing is necessary because the cores in the 0 state produce a small signal when "sensed" and because many of the cores in each mat receive half-selected pulses. The total sum of the noise can be considered a "delta noise", which appears at the early portion of the core selection time. The noise, generated by the half-selected cores, ceases shortly after the half-select pulses are started. Therefore, the Sense Amplifier is strobed during the latter part of the READ time, when the output resulting from a selected core-reversing state is highest in proportion to the noise from half-selected cores (maximum signal-to-noise ratio). Because the delta noise is confined to a smaller amplitude with respect to ground, the slice control ensures that any sampling of the 1 state occurs beyond the noise level amplitude. Thus, there are two methods of avoiding

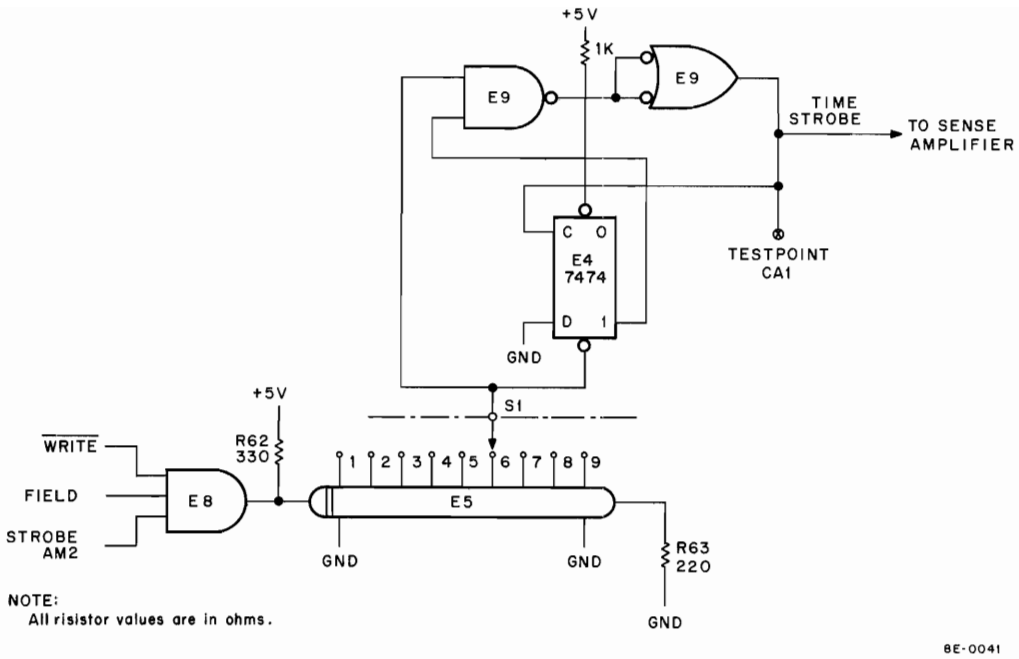
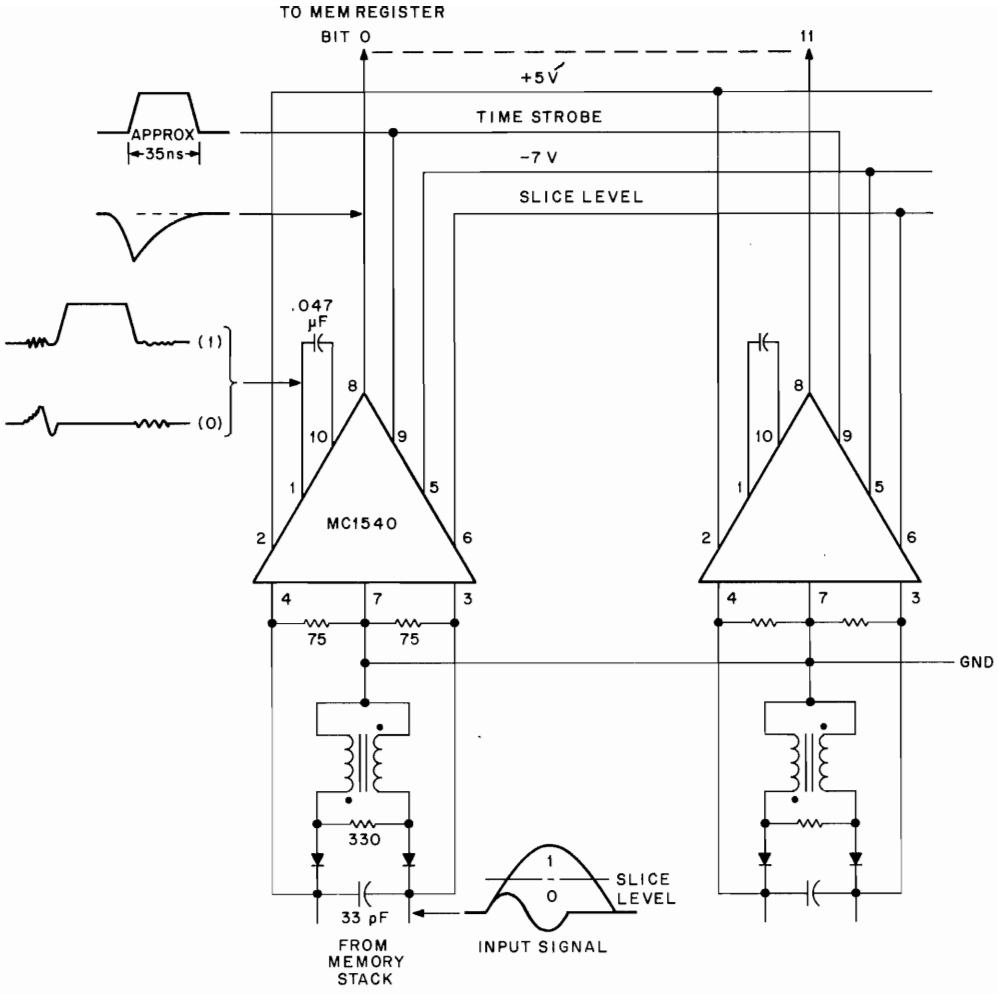


Figure 3-55 Strobe Control Circuit

the delta noise: (a) sample beyond the noise level amplitude, and (b) sample after the noise pulse. The delta noise is a direct function of the switching of the cores. For a 0, the Sense Amplifier senses a negligible change; a delta noise occurs but is not sensed, because STROBE is applied after the noise has settled down. STROBE is factory adjusted so that sampling clears the delta noise pulse, but does not clear it so far that the amplitude of a 1 is missed. This adjustment is in increments of 10 ns in a range of 30 to 40 ns. STROBE can be adjusted at the time-delay switch shown in Figure 3-55. However, the switch positions should not be changed until the diagnostic procedures indicate that STROBE timing is not properly synchronized. There are six distinct values on this switch in 10 ns increments. The switch is connected to a tapped delay line located on the Sense/Inhibit board. At CA1, a test point is available if any troubleshooting is necessary. The waveform is illustrated in Figure 3-56, corresponding to pin 9 of the Sense Amplifier; the sense line waveform at pin 10 is also shown. During the 1 state, the top portion is sliced off by the slice control input.

The balun transformer shown in Figure 3-56 performs an equalizing function for the inhibit currents during a WRITE operation. The Sense/Inhibit line is constructed so that one end of the wire is connected to one leg of the balun transformer, and the other end of the wire is connected to the other leg of the transformer. The inhibit output is tapped in the middle of this wire, thus forming a Y-type of connection. During the WRITE portion of the memory cycle, it is necessary to apply an equal amount of current through both legs of the Sense/Inhibit line. However, because the resistance on each leg is not exact (approximately 3Ω), it is possible to have 20 percent more current on one leg than the other. The balun transformer functions to make up the difference in current so that both legs are equalized. When the inhibit current is removed, a voltage backswing is prevented from entering the amplifier by the presence of the diodes. During the READ portion of the memory cycle, both ends of the diodes are at ground level and, therefore, back-biased. During the WRITE portion of the memory cycle, these diodes are forward-biased and, therefore, the transformer immediately begins balancing the currents.



NOTE:
All resistor values are in ohms

Figure 3-56 Sense Amplifiers

3.27.10 Memory Register

The Memory Registers (Figure 3-57) retain the information strobed out of the Sense Amplifiers until a CLEAR L signal is received during the first 50 ns of the next READ operation. The output gates, controlled by the READ MEM signal, drive 1s and 0s into the Inhibit Driver load gates. The flip-flops are termed "Sense flip-flops" and are set when there is a 1 (negative-going pulse) on the output of the corresponding Sense Amplifier. READ MEM is enabled only when MD DIR L is low.

3.27.11 Inhibit Driver Load Gates

The Inhibit Driver Load Gates (Figure 3-58) control the WRITE operation. During READ, the contents of the sense lines are placed on the MD lines. With FIELD (active) and INHIBIT (active), the contents of the MD lines are gated into the Inhibit Drivers. INHIBIT is generated in the Timing Generator only during the WRITE portion of the memory cycle.

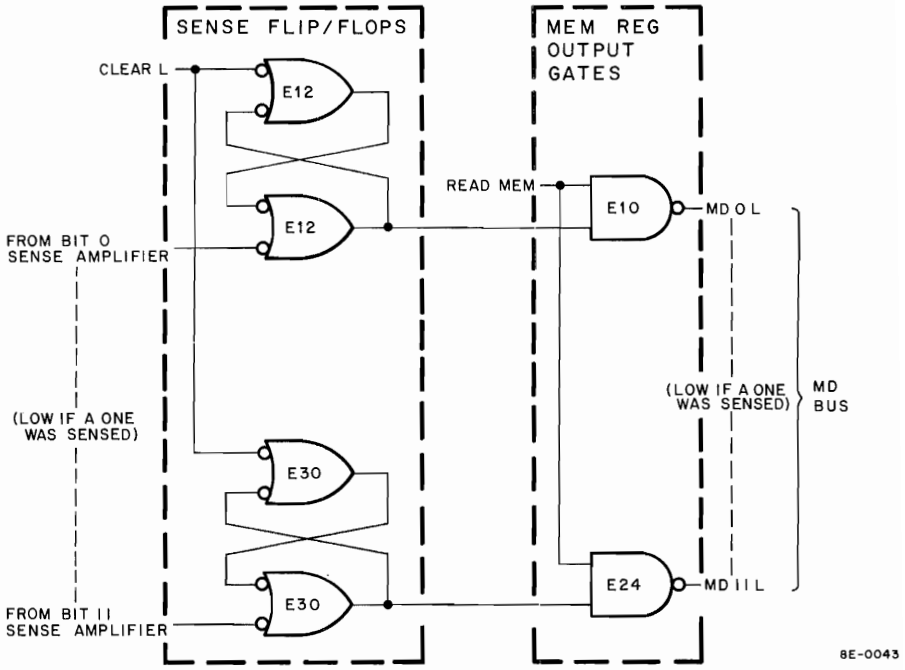


Figure 3-57 Memory Register

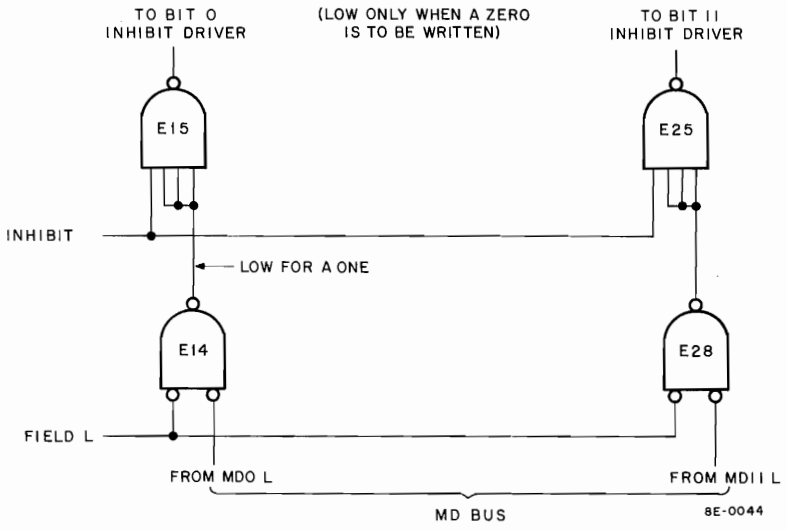


Figure 3-58 Inhibit Driver Load Gates

The MD lines receive data from the Sense flip-flops. When a FETCH or DEFER state is being processed, MD DIR L is made low and the memory cycle is a fast cycle (1.2 μs). This allows the content of the Sense flip-flops to be gated out to the Inhibit Driver load gates during WRITE and, subsequently, applied to the Inhibit Drivers. When data is to be written into memory from the MB Register, memory cycle timing is 1.4 μs and MD DIR L is high during the WRITE portion of the memory cycle. The Sense flip-flops are then made inactive, and the Inhibit Driver input gates look at only the MB Register. If data break is used, data is transferred immediately from a peripheral to the MB Register and gated into memory during the current memory cycle. During most other types of transfer operation, data must be transferred from the AC Register to the MB Register and applied to the Inhibit Driver input gates.

3.27.12 Inhibit Drivers

Inhibit Drivers (Figure 3-59) apply inhibit current to the selected core when a 0 is to be written. Each of the 12 drivers receives either a positive level (for a 1) or a ground input (for a 0) at the 1:1 input transformer. During a 0 output of any Inhibit Driver load gate, the transistor-base side of the transformer secondary is positive with respect to the emitter side. This forward bias turns the transistor on, allowing inhibit current to pass through and be applied to the selected core. Because the inhibit current direction is opposite to the write select current, a half-select condition results and the core remains in the 0 state. During a 1 output of any one Inhibit Driver input gate, the transistor-emitter at the same potential as the base and the transistor does not conduct. The full select current is then applied to the corresponding core, which results in a 1 state. The Inhibit Driver acts as a relay solenoid driver. It consists of an inductor, a resistor, and a switching transistor. When the transistor is turned on, the Inhibit line current is determined by the transistor emitter circuit. When the switch turns off, the energy stored in the inductor creates a back EMF that can damage the transistor circuit. The diode-to-ground at the collector output is used to protect the transistor from this unwanted backswing condition.

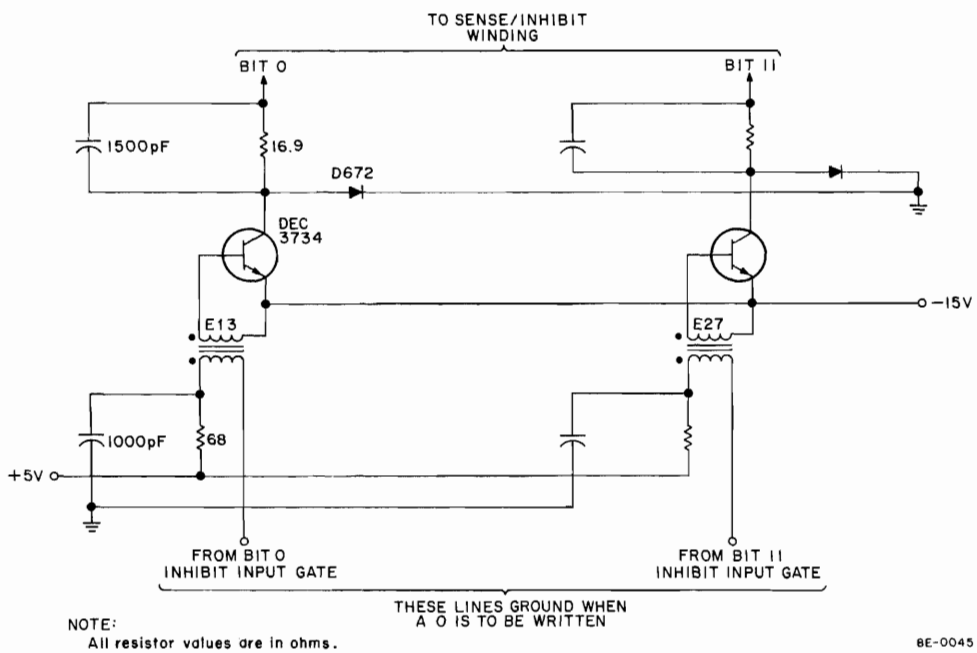


Figure 3-59 Inhibit Drivers

3.27.13 Current Control Circuit

The Current Control circuit (Figure 3-60) controls the current level in the X- and Y-select lines. The control circuit operates on a +5V and -15V supply. The output of the X- and Y-current sources (Figures 3-42 and 3-43) is a voltage-regulated supply that varies with temperature changes. The temperature sensing is accomplished by the thermistor, located on the memory stack board. The two jumpers are factory installed to control the preset X- and Y-current reference point.

3.27.14 -7V Supply and Slice Control Circuits

The -7V Supply and Slice Control circuits (Figure 3-61) provide a voltage slice level to the Sense Amplifier (Figure 3-56) and a regulated -5 Vdc output to the Sense Amplifier. The slice level is controlled by jumpers SLA and SLB, which are factory installed.

3.28 MEMORY TRANSFER CONTROL LOGIC

Memory transfer control is accomplished by signal MD DIR L. When MD DIR L is low, the content of the Memory Register, containing information from the READ operation, is gated out to the MD BUS. When MD DIR L is high, the content of the MB Register is gated out to the MD BUS for deposit in memory during the WRITE operation. When the processor directs memory to write back into memory the word retrieved during READ (manipulating signal MD DIR L), MD DIR L remains low during the WRITE operation. The content of the Memory Register is on the MD BUS; consequently, the same word is written back into memory. This procedure always applies during FETCH and DEFER (NON-AUTOINDEX).

3.28.1 Transfer Control During FETCH, DEFER, or EXECUTE States

The memory transfer control logic for FETCH, DEFER, or EXECUTE states is illustrated in Figure 3-62. A CLEAR L signal is generated by timing 100 ns after the start of TS1. This resets E19, which asserts MD DIR L. The flip-flop remains unchanged until TP2 is received as a clock input. If the major state is FETCH, a low will be clocked into the data input of the flip-flop, and E19 remains unchanged until TP2 of the next cycle. If the major state is DEFER (NON-AUTOINDEX), a low will be clocked into the data input of the flip-flop, and E19 remains unchanged. Thus, in both cases, the data from the Memory Register is re-deposited in memory.

If the major state is DEFER and AUTOINDEX (MA0–7 L equals 0 and MA8 L equals 1), a high is clocked into the flip-flop, and E19 is set. A low into E27 causes MD DIR L to go high, and memory receives the data from the MB Register.

If the major state is EXECUTE, a high is clocked into the data input of the flip-flop, and E19 is set; this condition, as in the previous case, causes MD DIR L to be high.

3.28.2 DMA State, Manual Operation Transfer Control

MD DIR L is high at TP2 unless pulled low by the Memory Transfer Control logic in the Programmer's Console (Figure 3-63).

Because FETCH or DEFER is not asserted, due to the DMA state, the Memory Transfer Control logic in the Timing Generator remains high, because no reset pulse is generated by timing. Either the LOAD ADDR or EXAM key, when depressed, will generate MD DIR L, which places the content of the Memory Register onto the MD BUS.

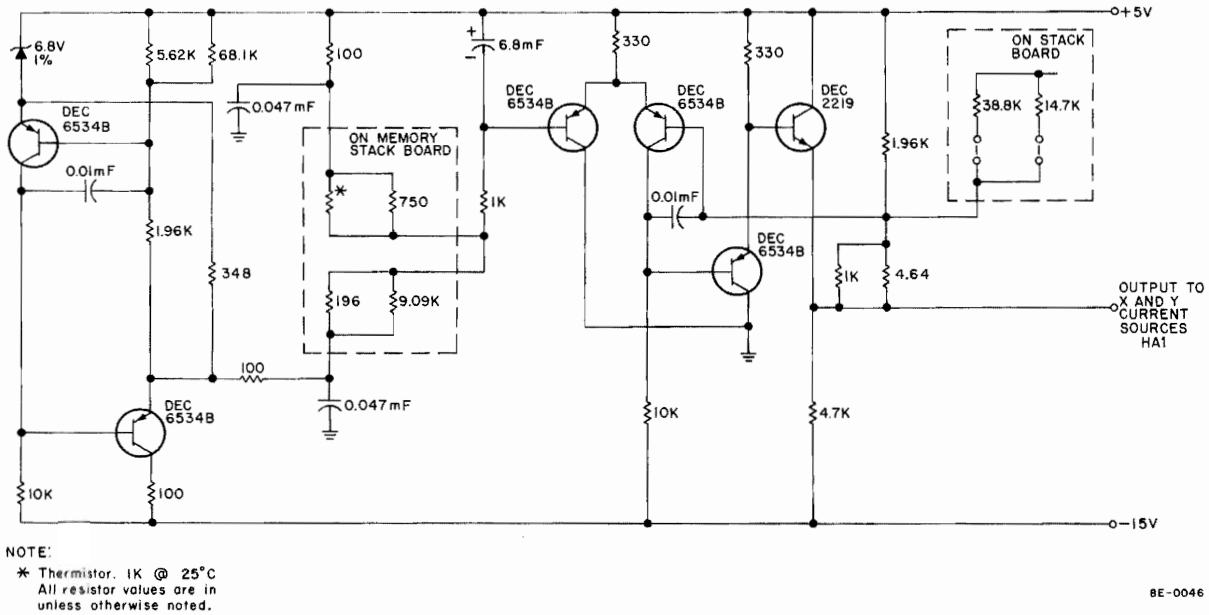


Figure 3-60 Current Control

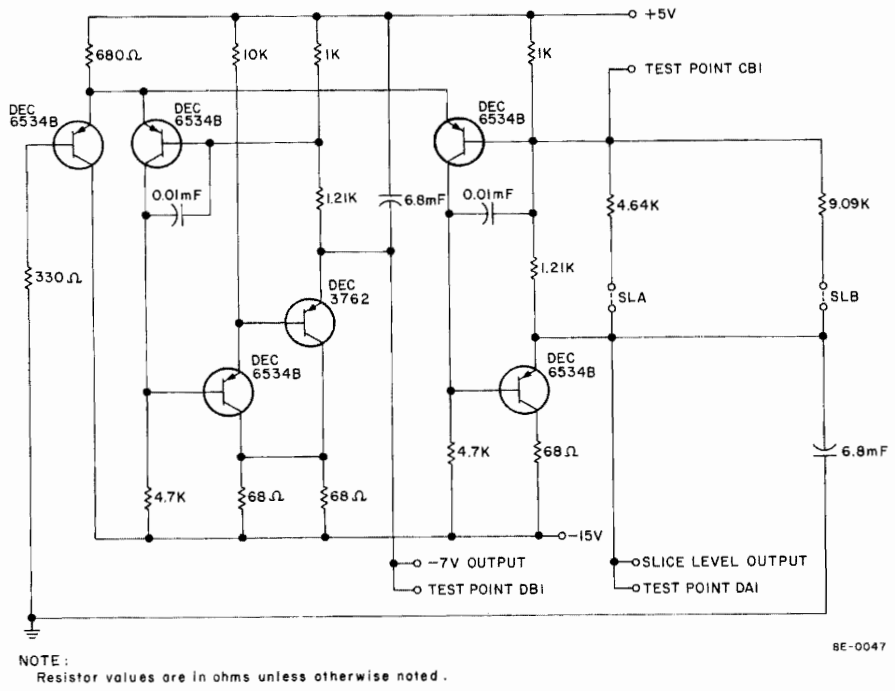


Figure 3-61 -7V Supply and Slice Control Circuits

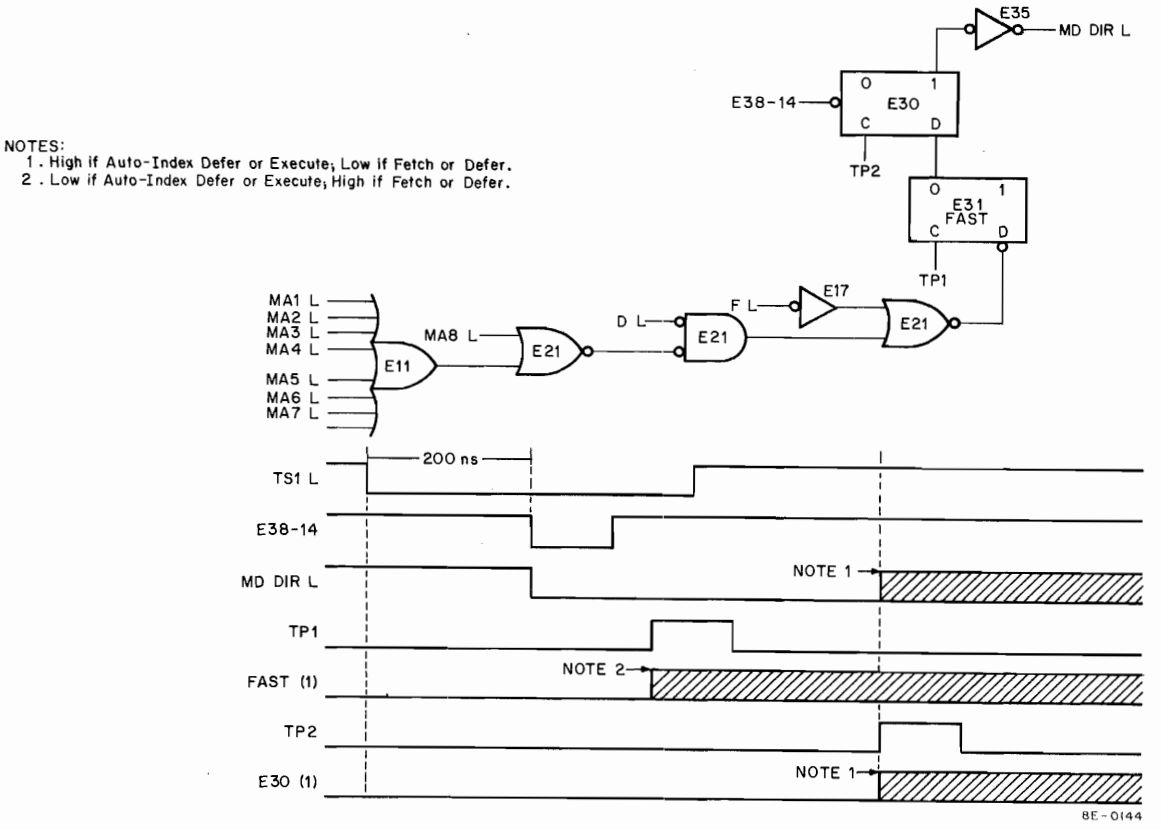


Figure 3-62 Memory Transfer Control Logic (FETCH, DEFER, or EXECUTE)

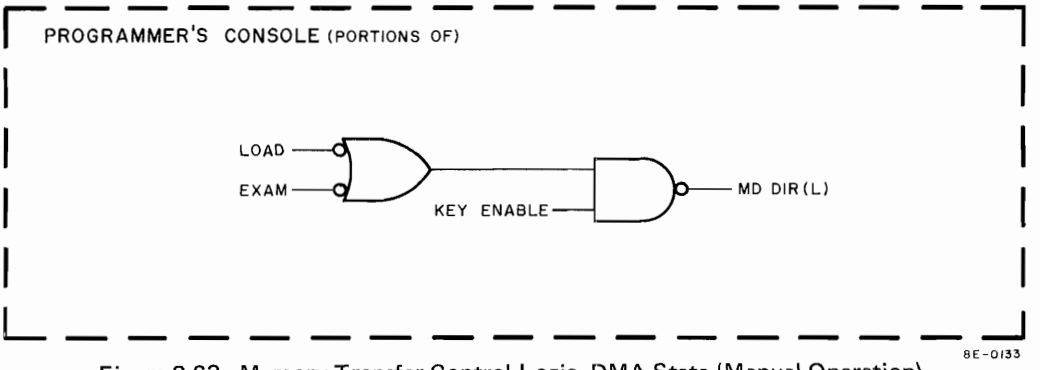


Figure 3-63 Memory Transfer Control Logic, DMA State (Manual Operation)

When data is deposited into memory, the data path is from the DATA BUS to the MB Register to memory. Thus, MD DIR L must go high so that the content of the MB Register can be gated out to the MD BUS.

3.28.3 DMA State, Data Break Operation

Each data break device contains Memory Transfer Control logic. MD DIR L will always be low except when:

a. Incrementing the word count (3-cycle data break device)

b. Incrementing the current address (3-cycle data break device)

c. Transferring data from the device to memory, or incrementing memory.

Refer to Volume 2, Chapter 10 of this manual for a detailed discussion of data break transfers.